

Virtex-II Pro Development Board Chaparral	
Avnet Design Services	
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Revision		
Zone	Rev.	Description
1A	A	Initial Revision
1A	B	Production Board (Rev. B)
	C	Fixed Spartan-1E Power Sequencing

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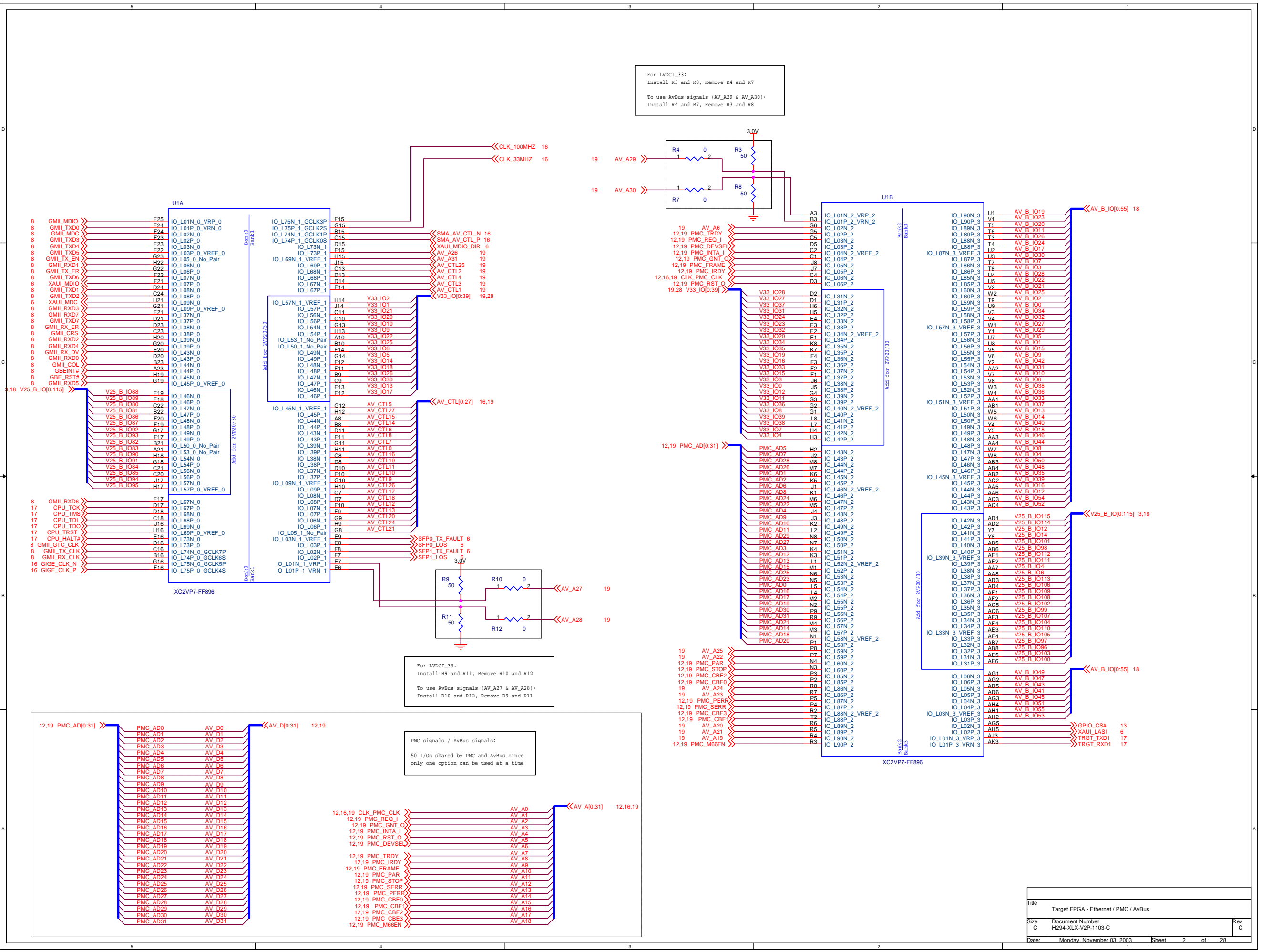
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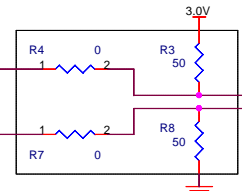
REVISION C

Avnet, Inc. Design Services Copyright 2002	
Title	Virtex-II Pro Development Board Cover Sheet
Size	Document Number
C	H294-XLX-V2P-1103-C
Date:	Monday, November 03, 2003 Sheet 1 of 28



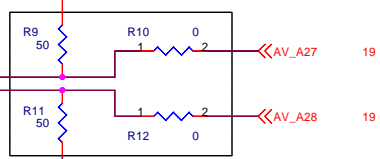
For LVDCI_33:
Install R3 and R8, Remove R4 and R7

To use AvBus signals (AV_A29 & AV_A30):
Install R4 and R7, Remove R3 and R8



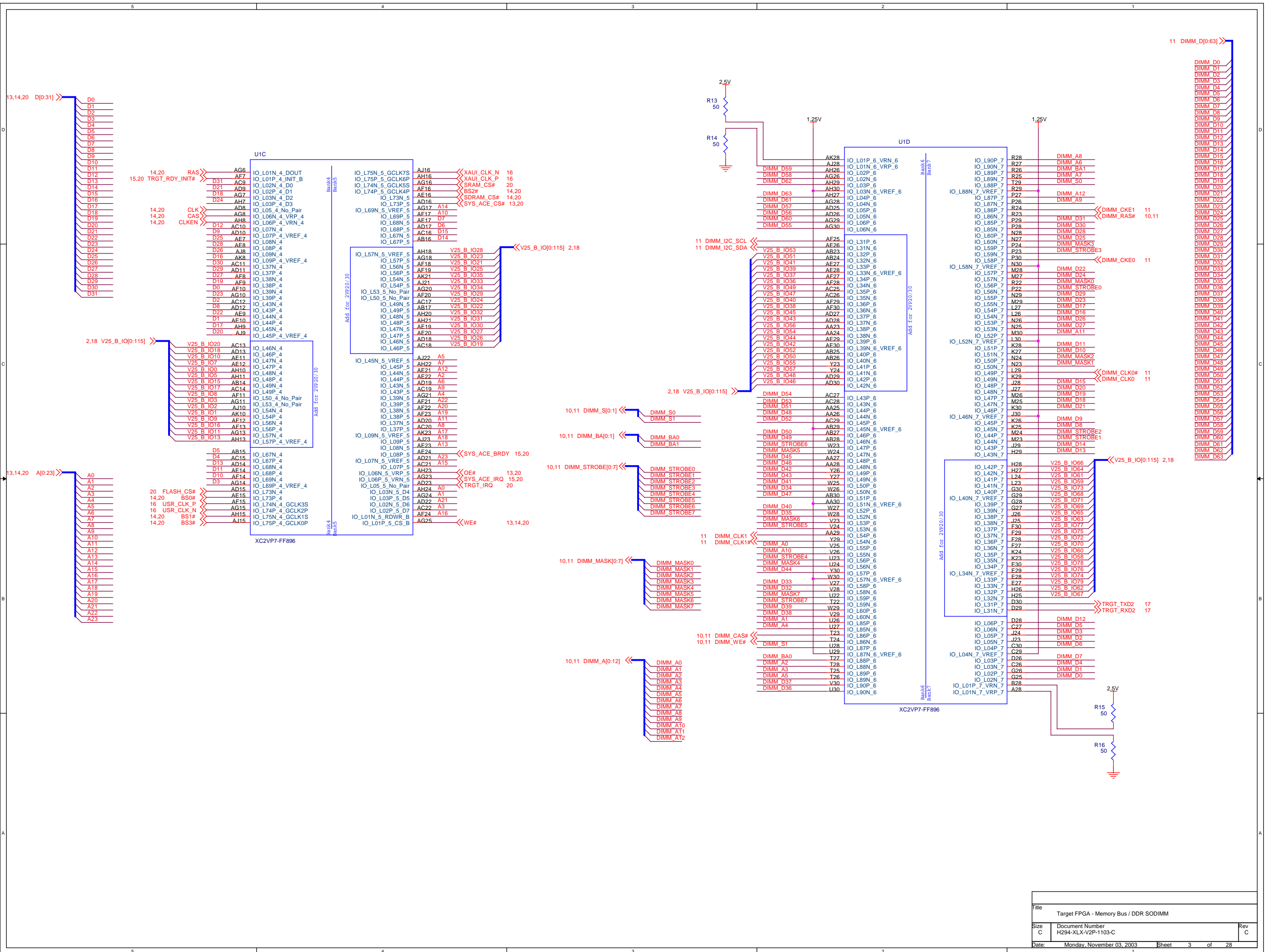
For LVDCI_33:
Install R9 and R11, Remove R10 and R12

To use AvBus signals (AV_A27 & AV_A28):
Install R10 and R12, Remove R9 and R11

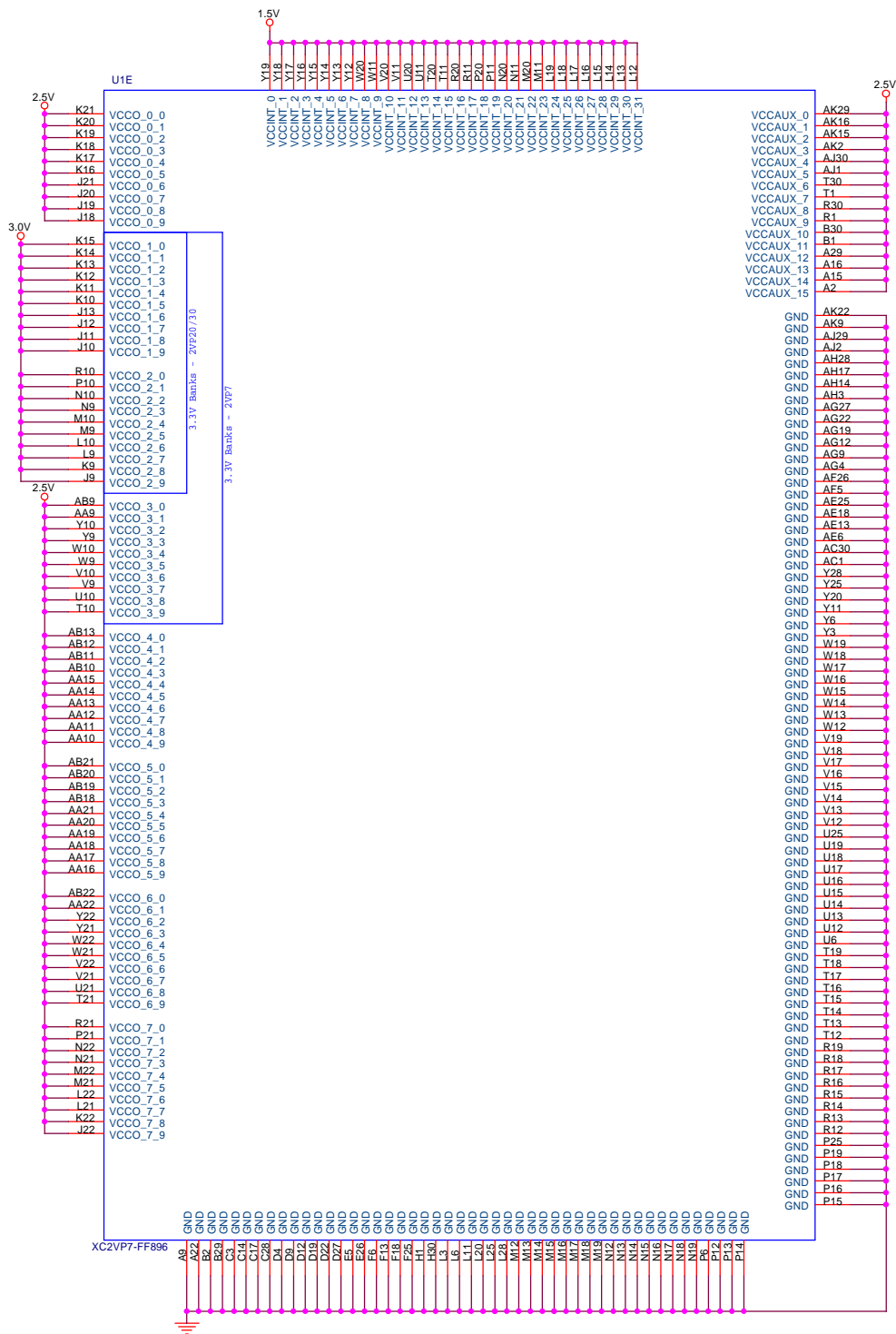
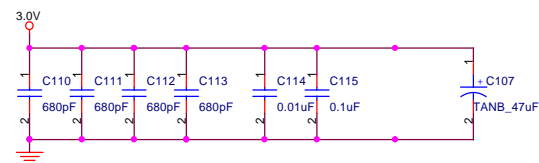
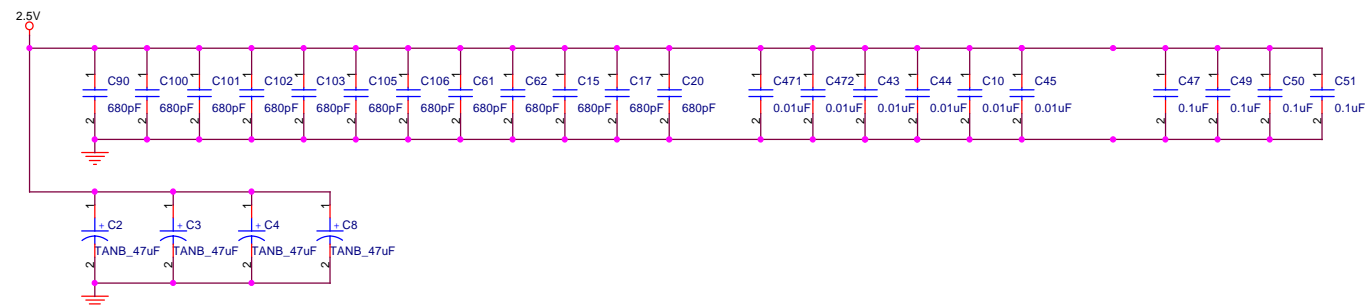
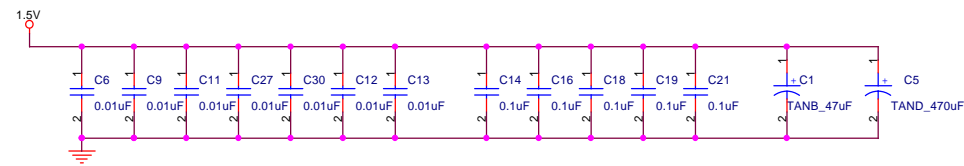


PMC signals / AvBus signals:
50 I/Os shared by PMC and AvBus since only one option can be used at a time

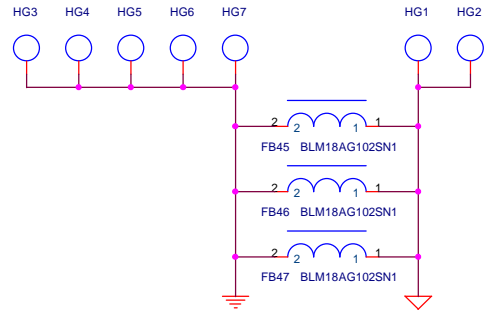
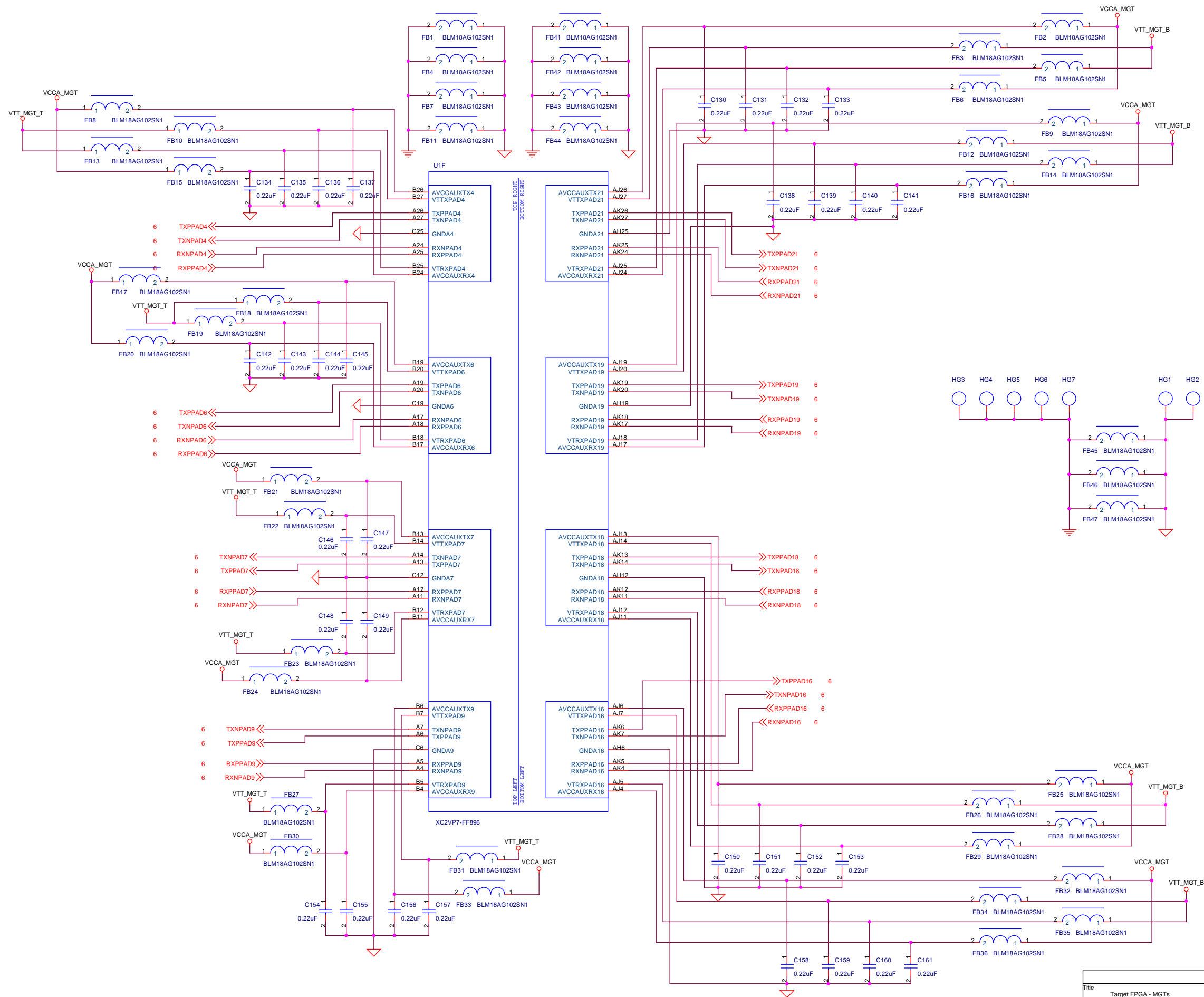
12,19 PMC_AD[0:31]	PMC AD0	AV D0	AV_A0
	PMC AD1	AV D1	AV A1
	PMC AD2	AV D2	AV A2
	PMC AD3	AV D3	AV A3
	PMC AD4	AV D4	AV A4
	PMC AD5	AV D5	AV A5
	PMC AD6	AV D6	AV A6
	PMC AD7	AV D7	AV A7
	PMC AD8	AV D8	AV A8
	PMC AD9	AV D9	AV A9
	PMC AD10	AV D10	AV A10
	PMC AD11	AV D11	AV A11
	PMC AD12	AV D12	AV A12
	PMC AD13	AV D13	AV A13
	PMC AD14	AV D14	AV A14
	PMC AD15	AV D15	AV A15
	PMC AD16	AV D16	AV A16
	PMC AD17	AV D17	AV A17
	PMC AD18	AV D18	AV A18
	PMC AD19	AV D19	AV A19
	PMC AD20	AV D20	AV A20
	PMC AD21	AV D21	AV A21
	PMC AD22	AV D22	AV A22
	PMC AD23	AV D23	AV A23
	PMC AD24	AV D24	AV A24
	PMC AD25	AV D25	AV A25
	PMC AD26	AV D26	AV A26
	PMC AD27	AV D27	AV A27
	PMC AD28	AV D28	AV A28
	PMC AD29	AV D29	AV A29
	PMC AD30	AV D30	AV A30
	PMC AD31	AV D31	AV A31



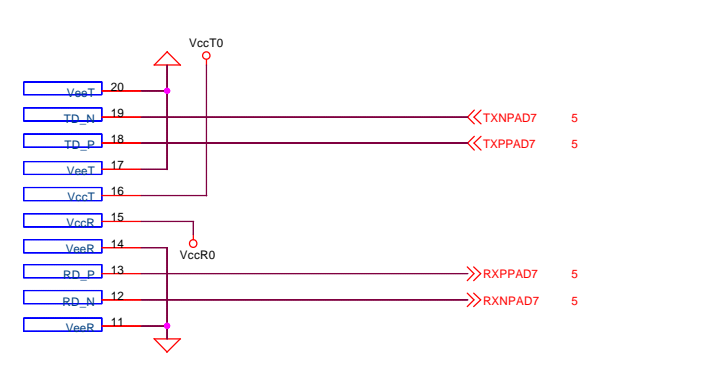
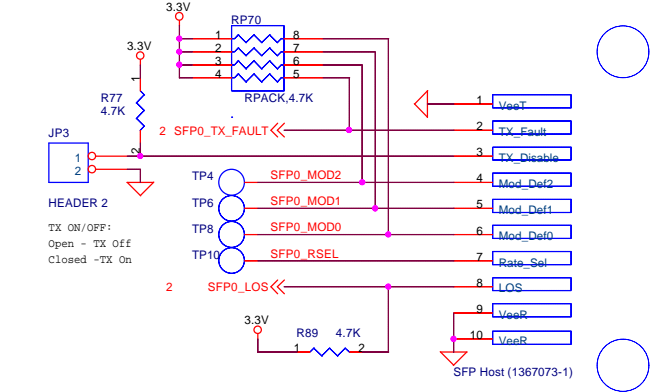
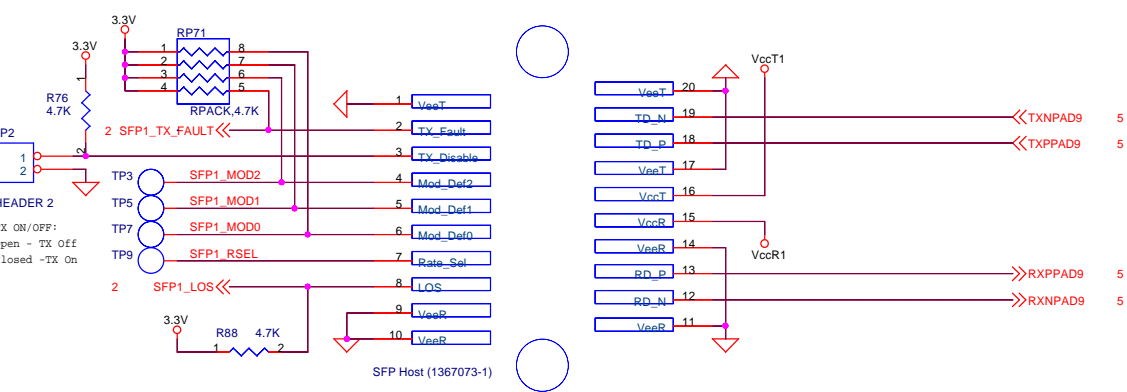
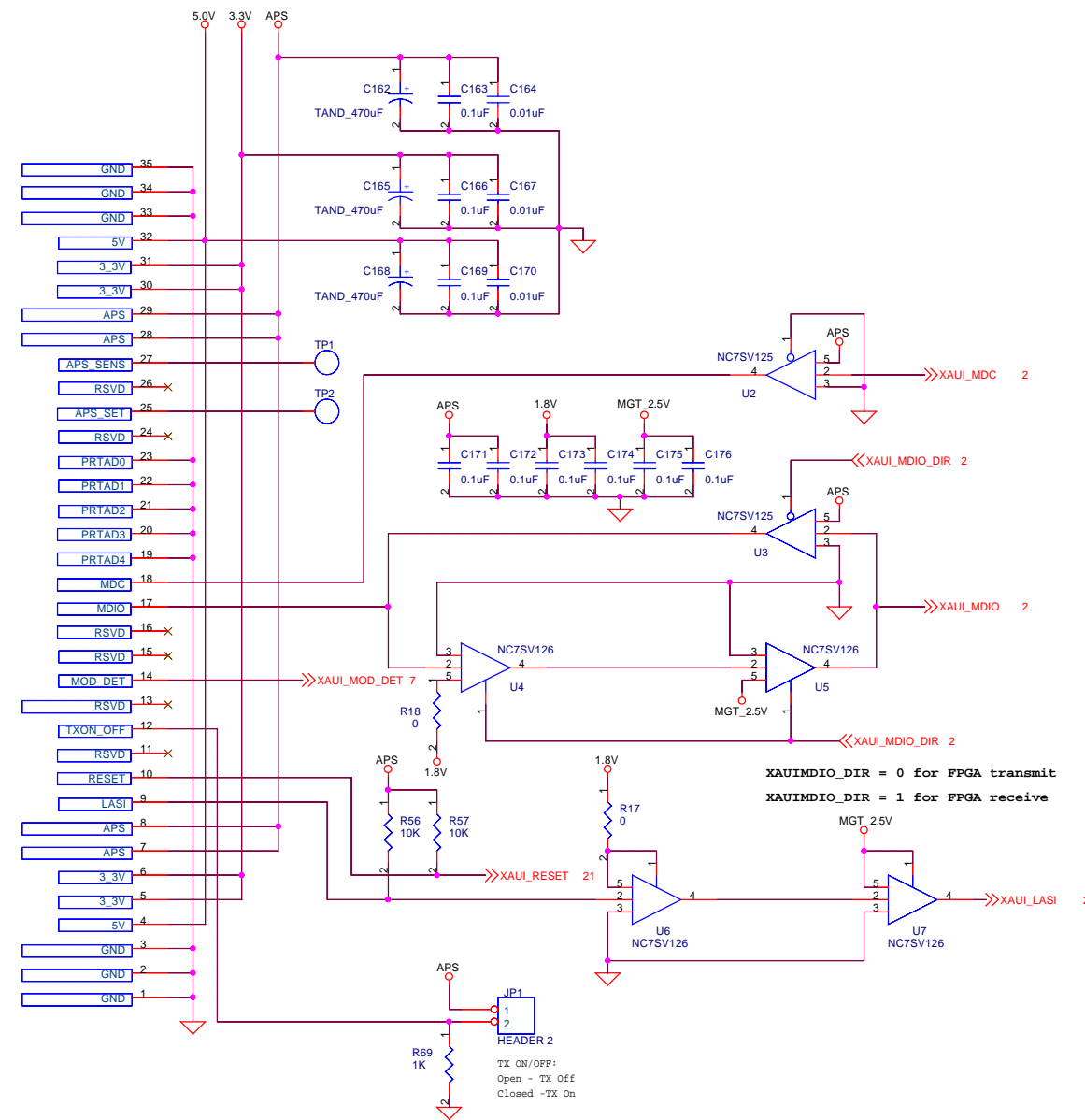
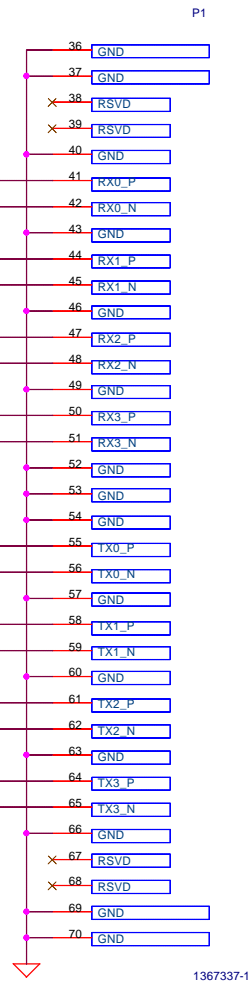
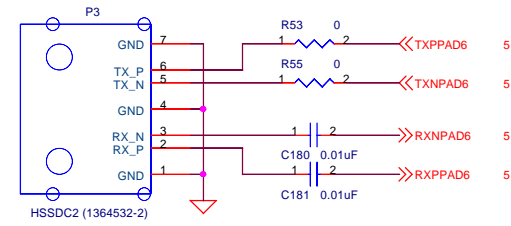
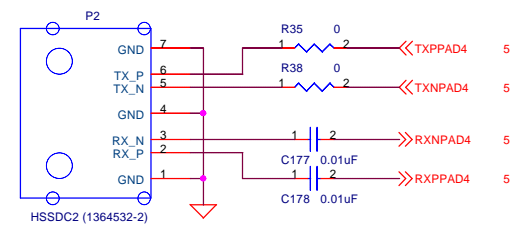
Title			Target FPGA - Memory Bus / DDR SODIMM		
Size	Document Number		Rev		
C	H294-XLX-V2P-1103-C		C		
Date:	Monday, November 03, 2003	Sheet	3	of	28



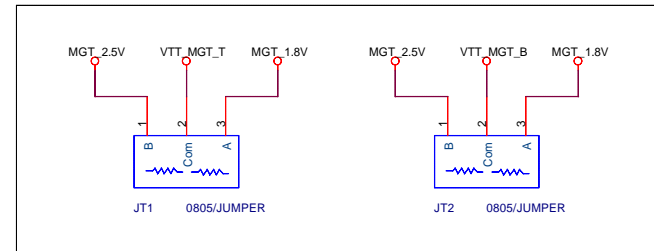
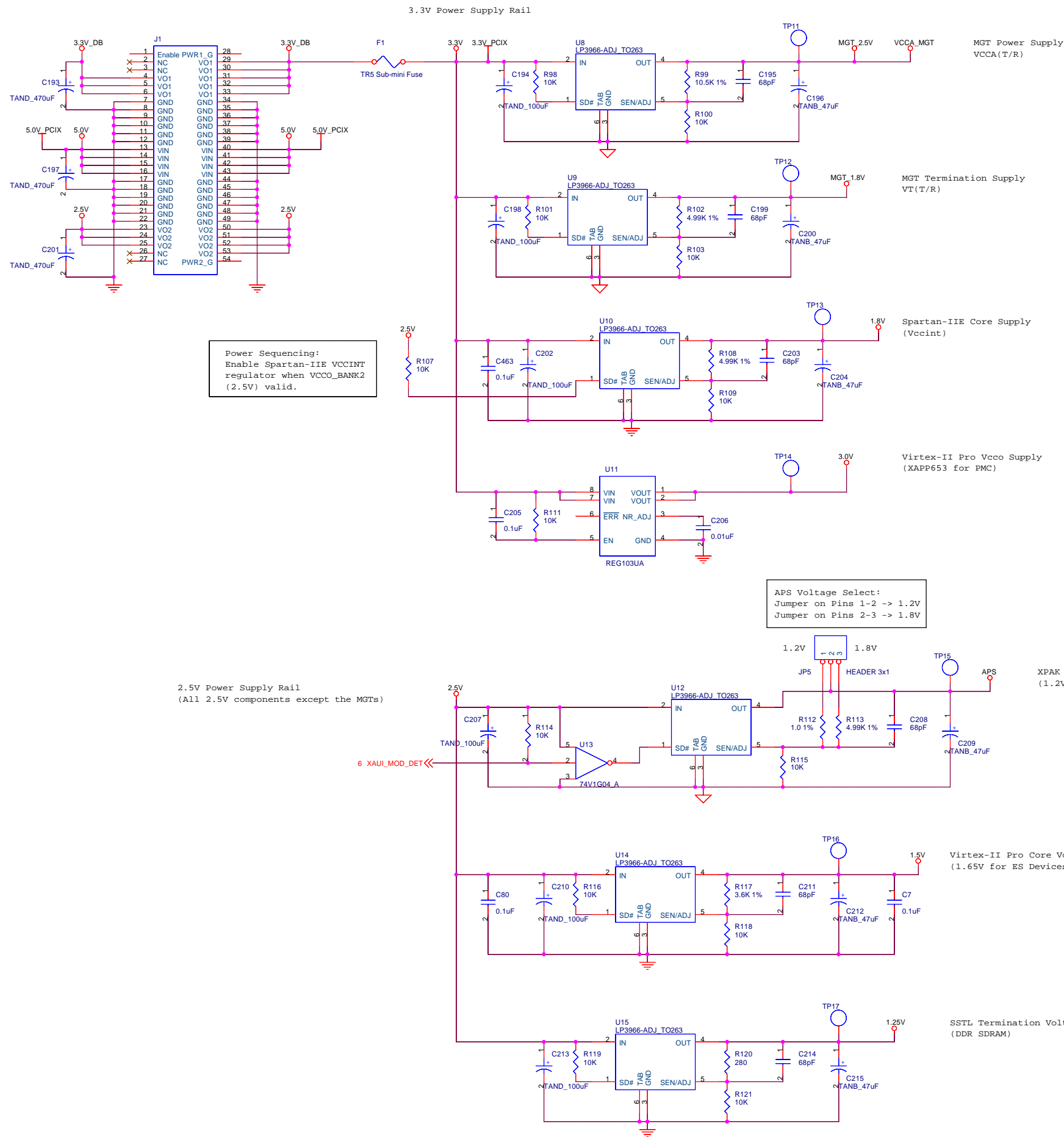
Title		
Target FPGA - Vint, Vcco, Vccaux		
Size	Document Number	Rev
C	H294-XLX-V2P-1103-C	C
Date:	Monday, November 03, 2003	Sheet 4 of 28



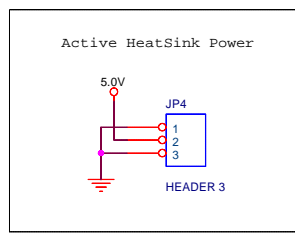
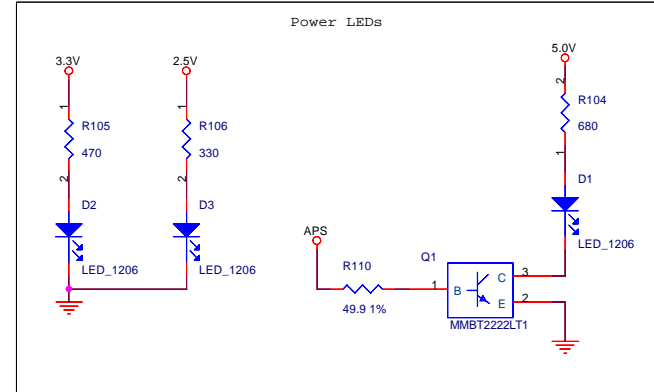
Title		
Target FPGA - MGTs		
Size	Document Number	Rev
C	H294-XLX-V2P-1103-C	C
Date:	Monday, November 03, 2003	Sheet 5 of 28



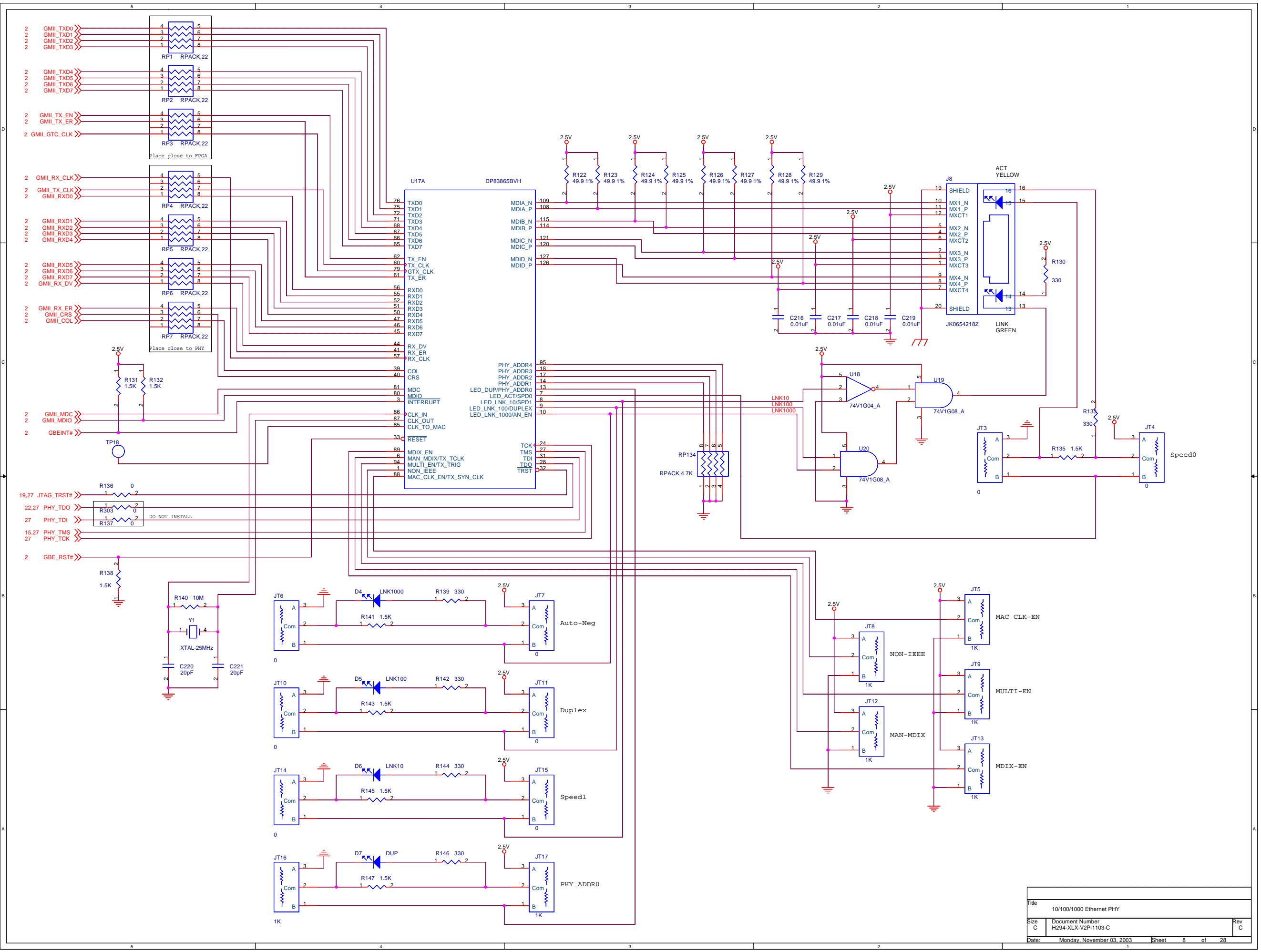
Title Target FPGA - MGT2		
Size C	Document Number H294-XLX-V2P-1103-C	Rev C
Date: Monday, November 03, 2003	Sheet 6	of 28



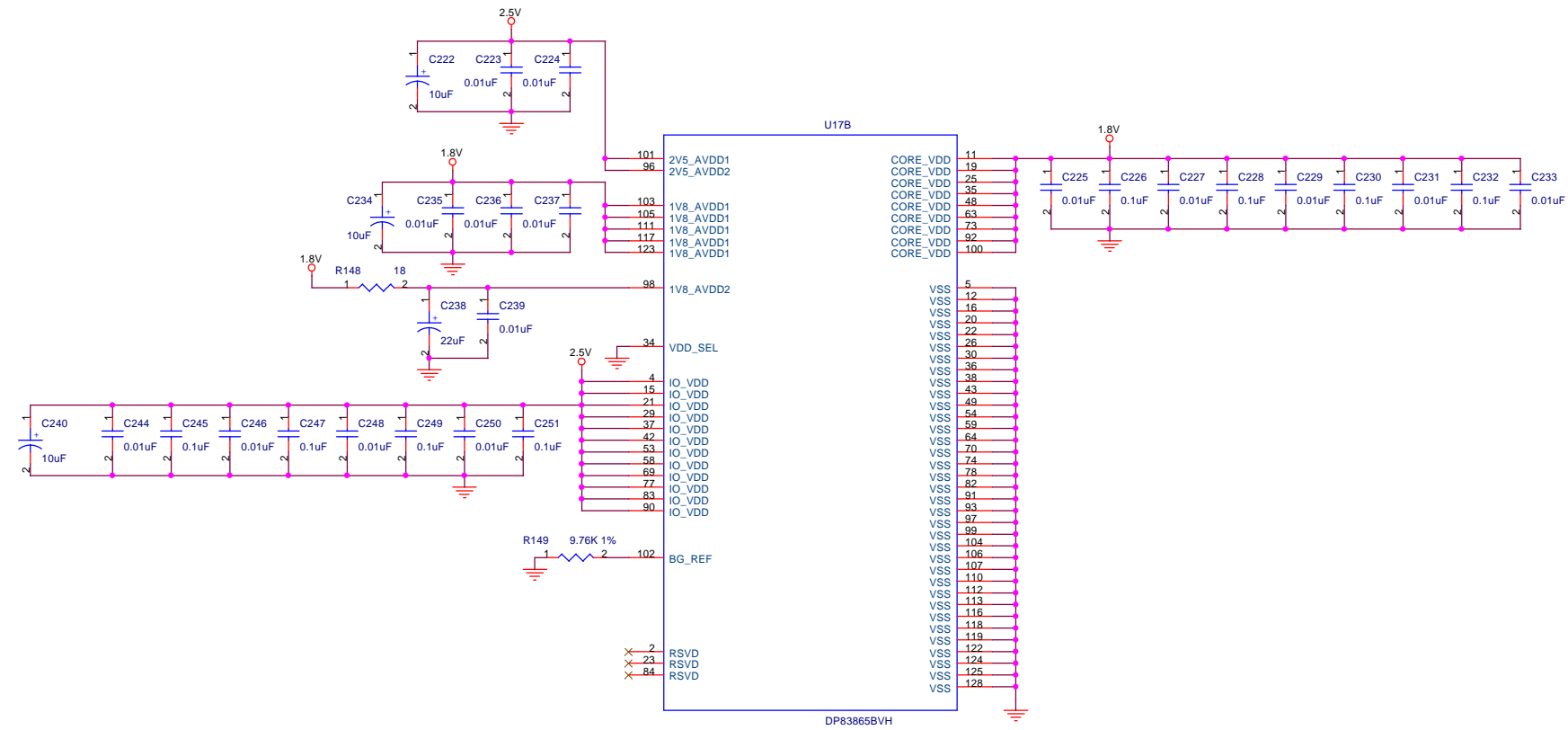
MGT Termination Voltage Select:
JT1 - Top Edge MGTs (HSSDC2 (x2) & SFP (x2))
JT2 - Bottom Edge MGTs (XPAK)



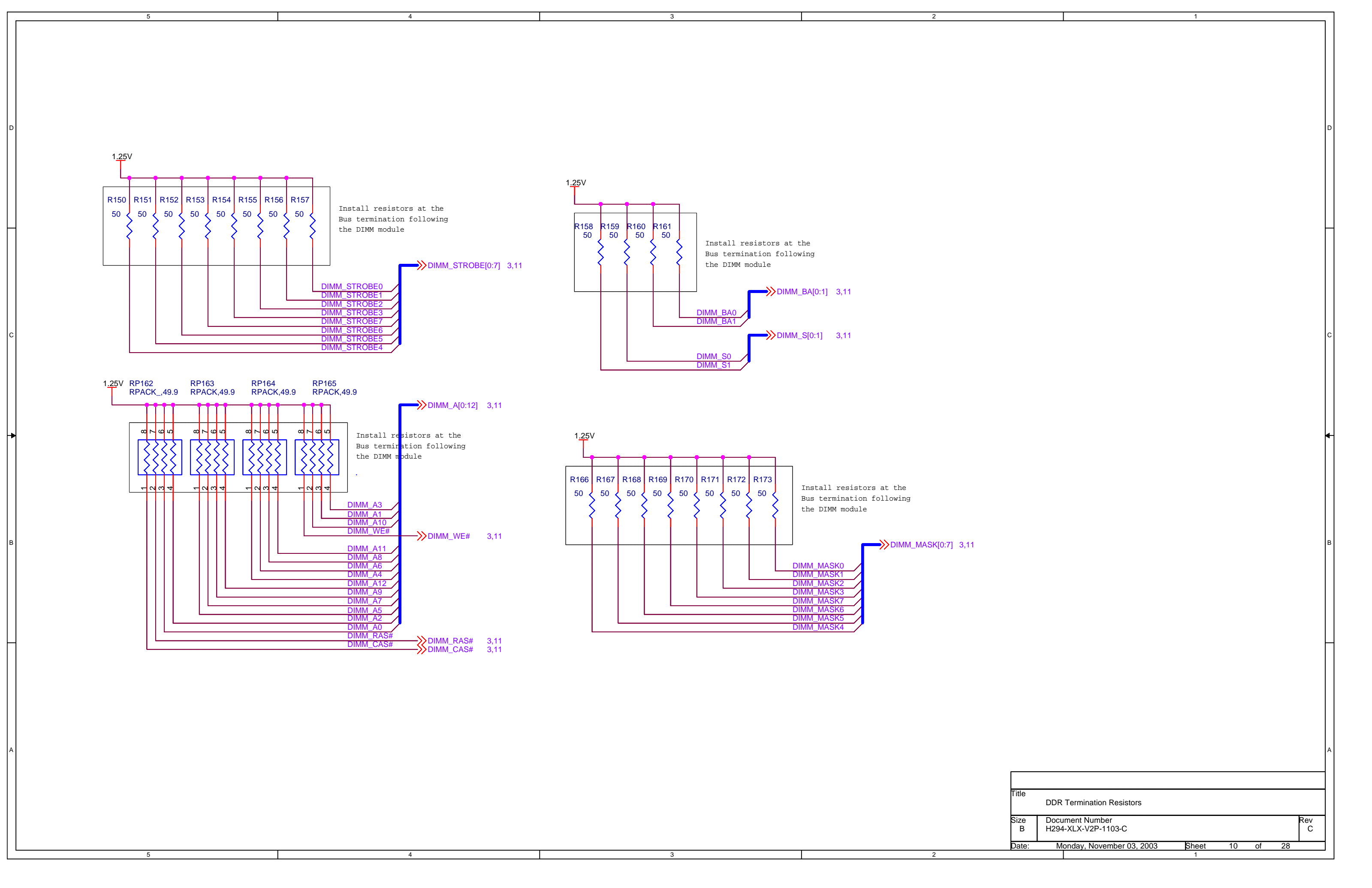
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Size	Document Number		Rev		
C	H294-XLX-V2P-1103-C		C		
Date:	Monday, November 03, 2003	Sheet	7	of	28



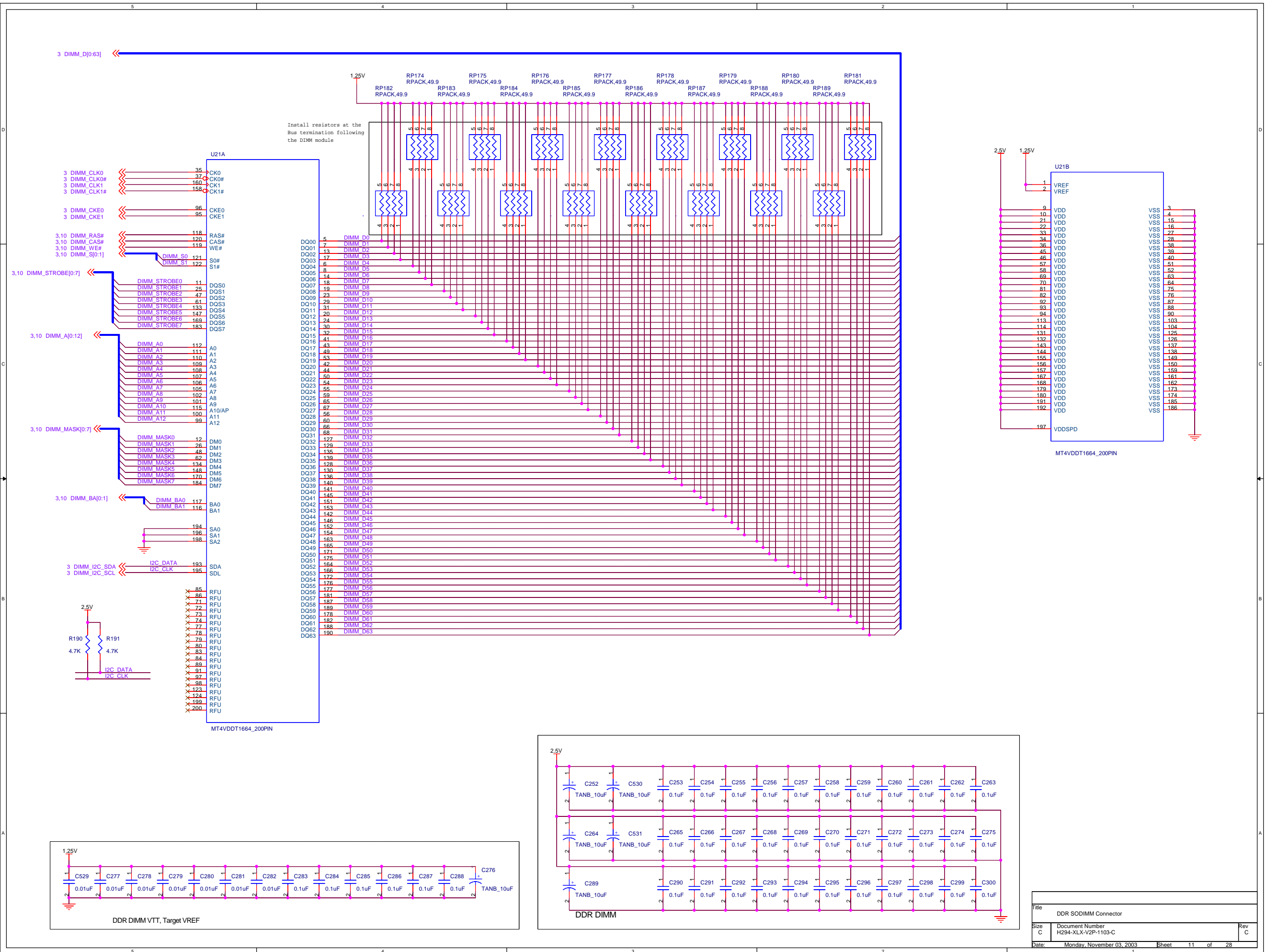
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10/100/1000 Ethernet PHY		
Size	Document Number	Rev
C	H294-XLX-V2P-1103-C	C
Date:	Monday, November 03, 2003	Sheet 8 of 28



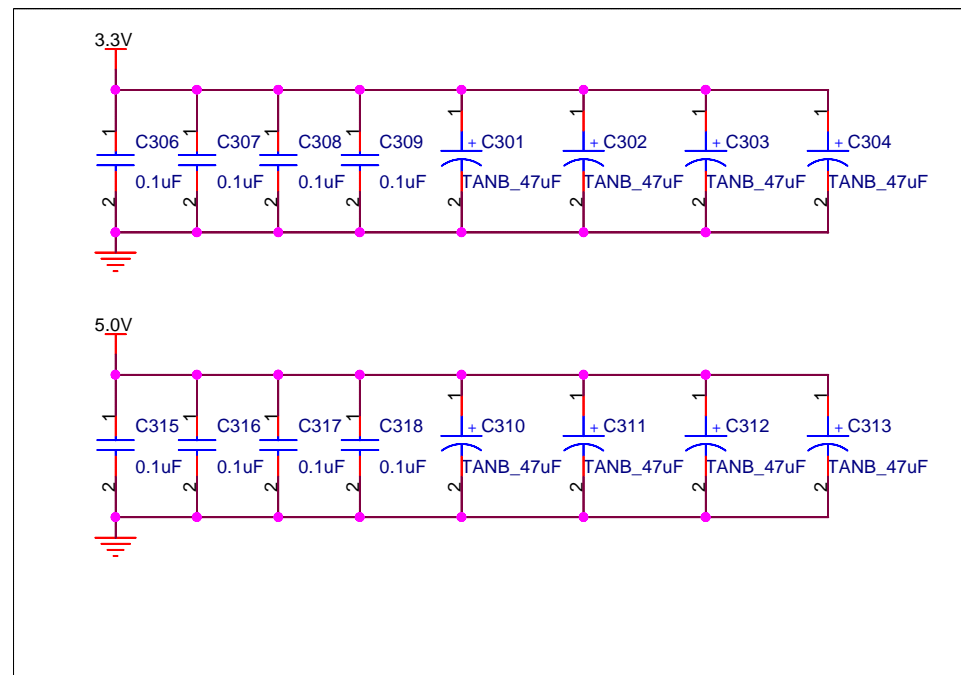
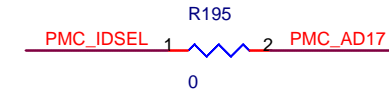
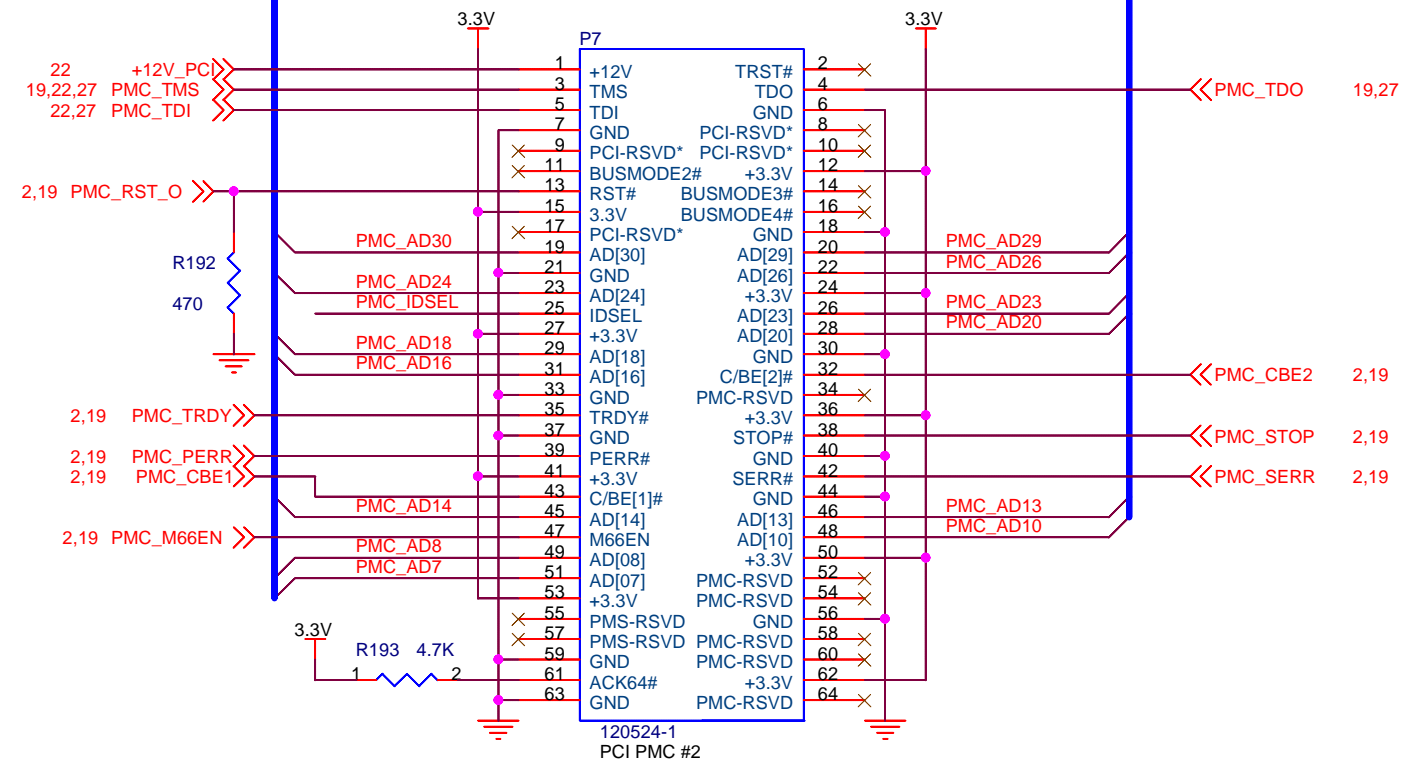
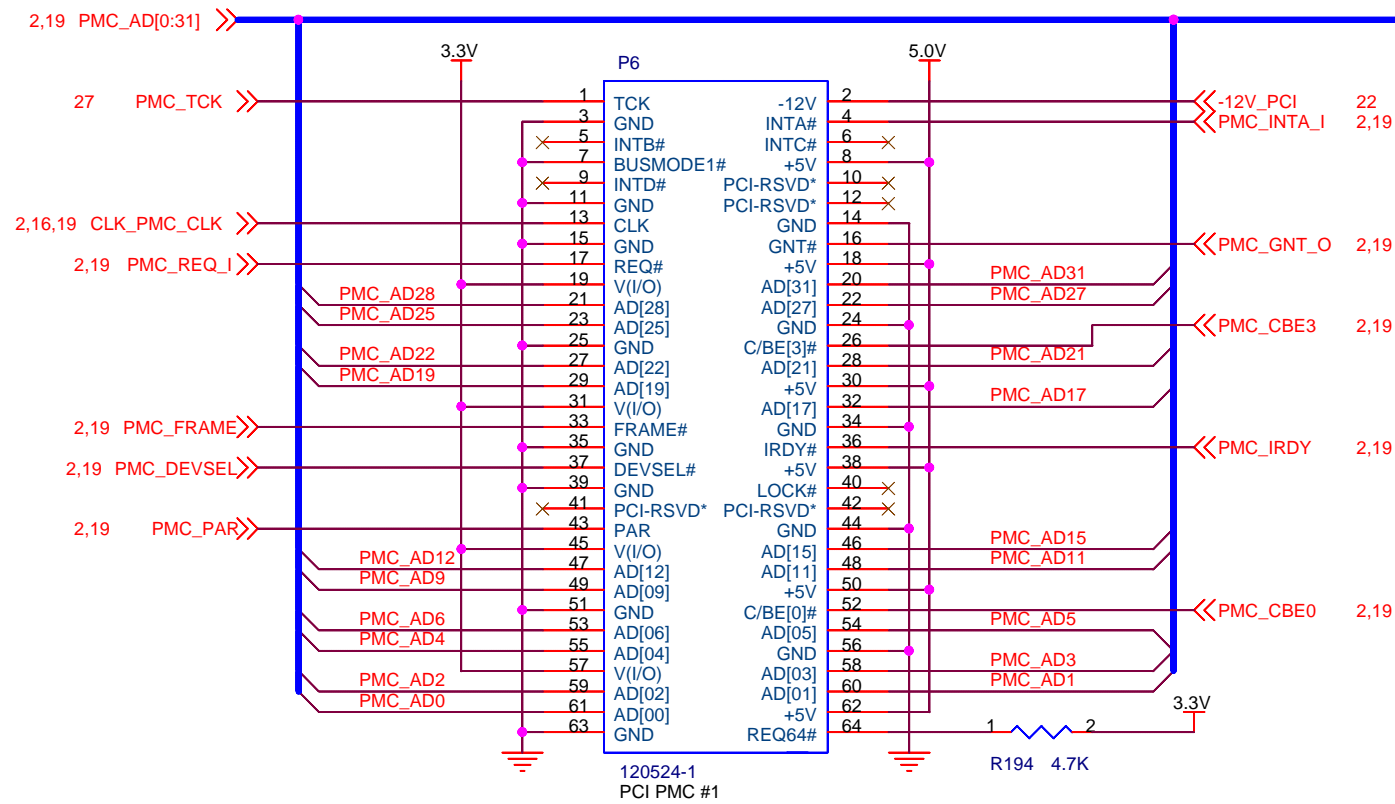
Title		
Ethernet PHY Power		
Size	Document Number	Rev
C	H294-XLX-V2P-1103-C	C
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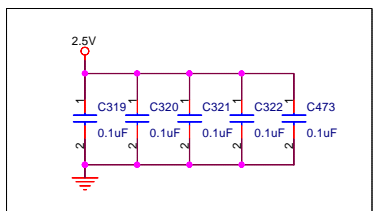
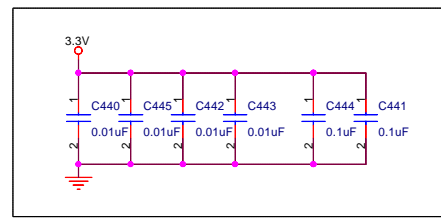
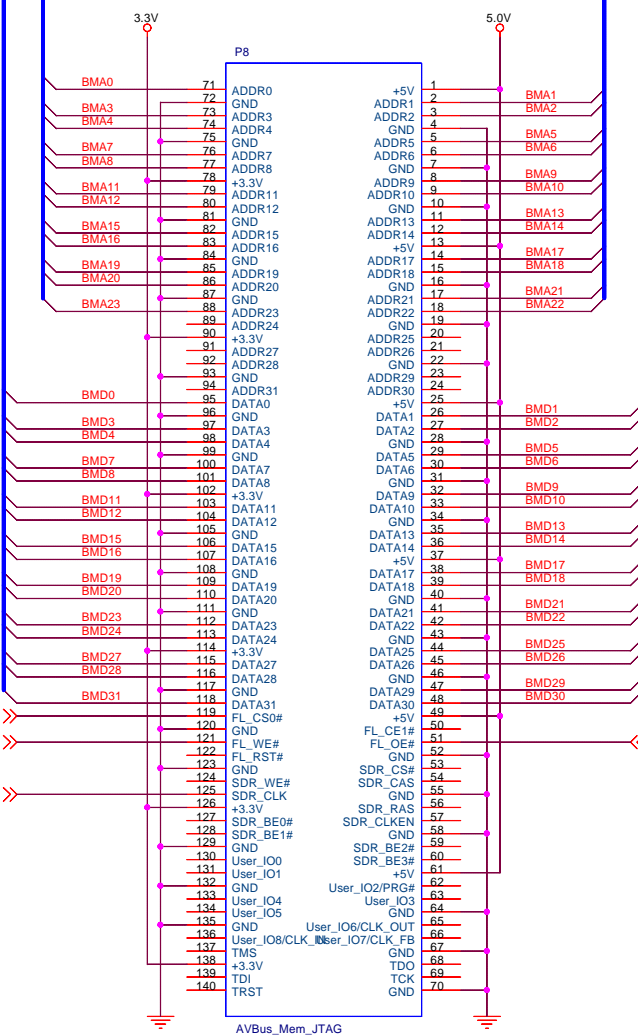
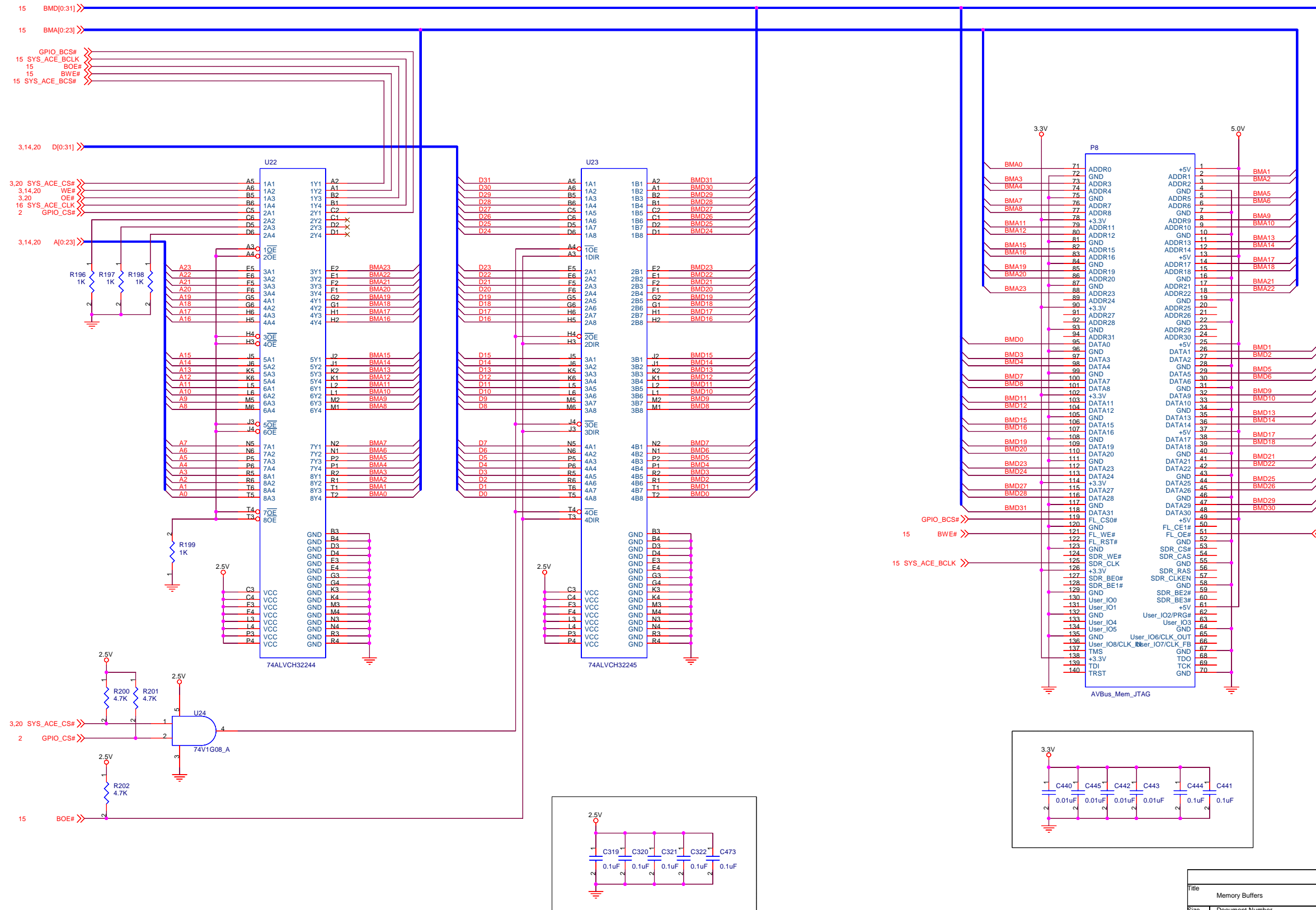
Title		
DDR Termination Resistors		
Size	Document Number	Rev
B	H294-XLX-V2P-1103-C	C
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Title			DDR SODIMM Connector		
Size	Document Number	Rev			
C	H294-XLX-V2P-1103-C	C			
Date:	Monday, November 03, 2003	Sheet	11	of	28

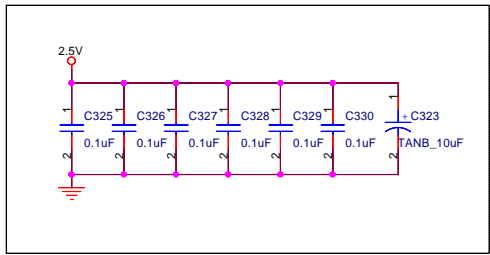


Title PMC Connectors		
Size B	Document Number H294-XLX-V2P-1103-C	Rev C
Date: Monday, November 03, 2003	Sheet 12 of 28	

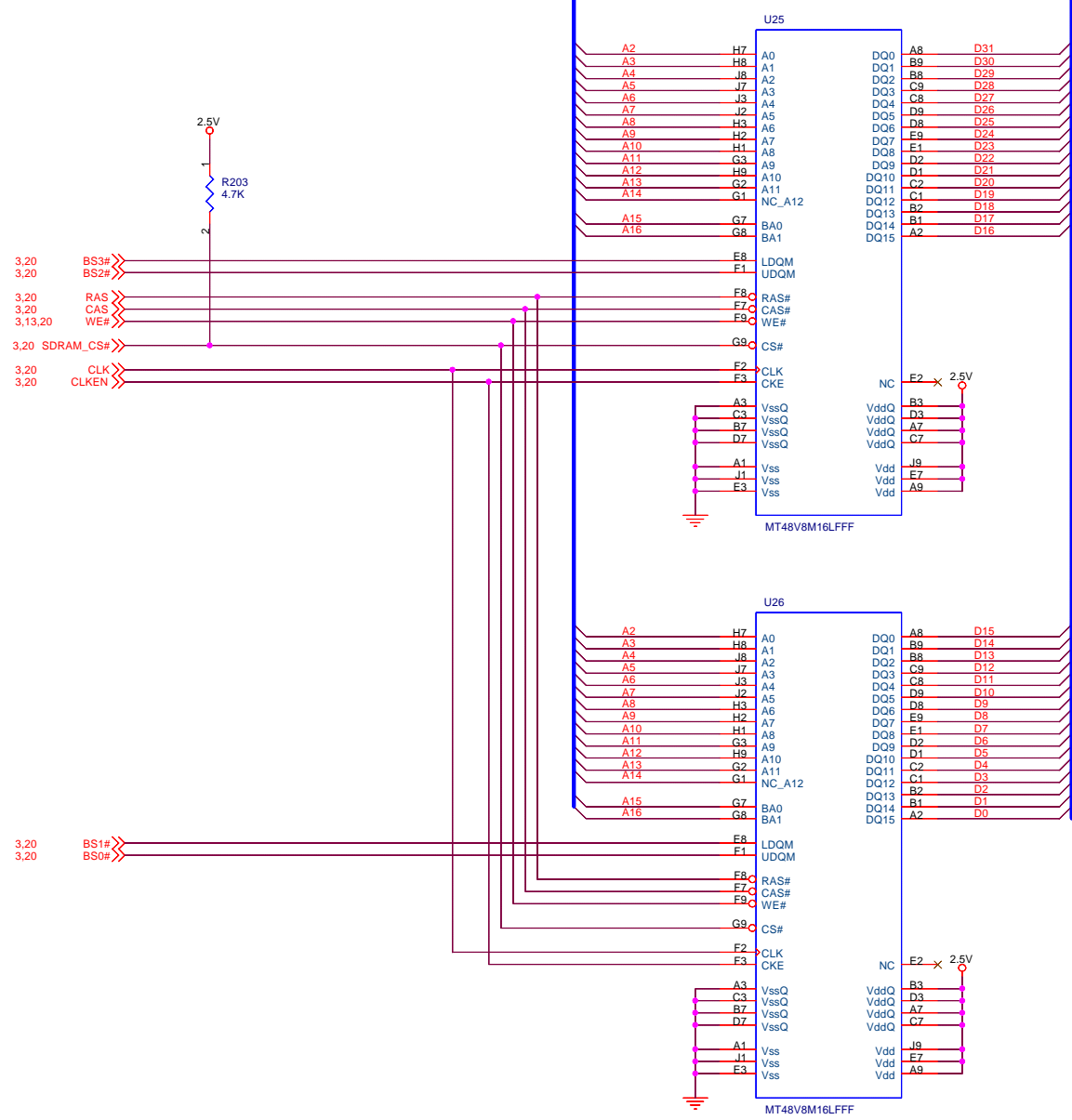


Title		
Memory Buffers		
Size	Document Number	Rev
C	H294-XLX-V2P-1103-C	C
Date:	Monday, November 03, 2003	Sheet 13 of 28

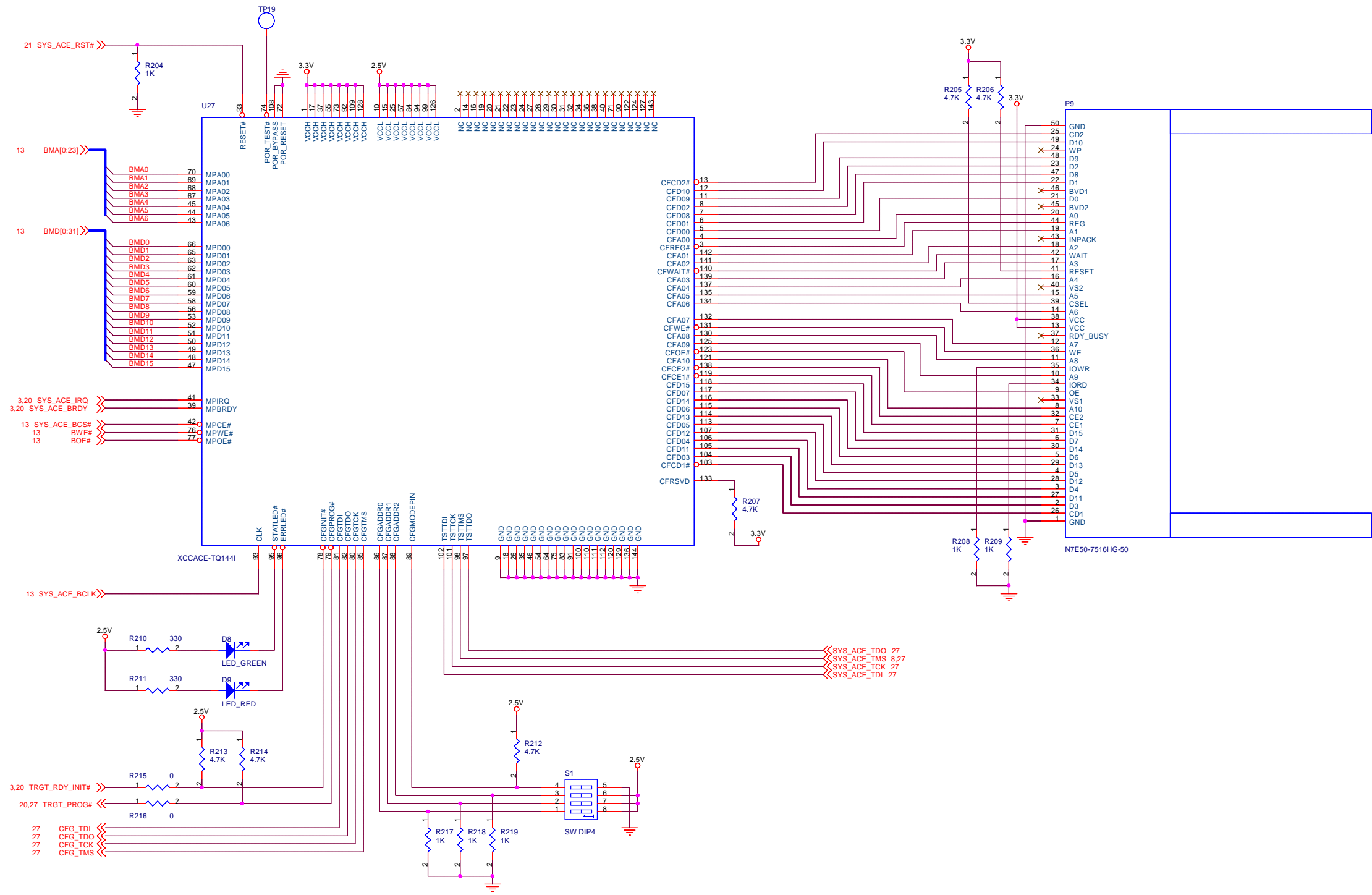
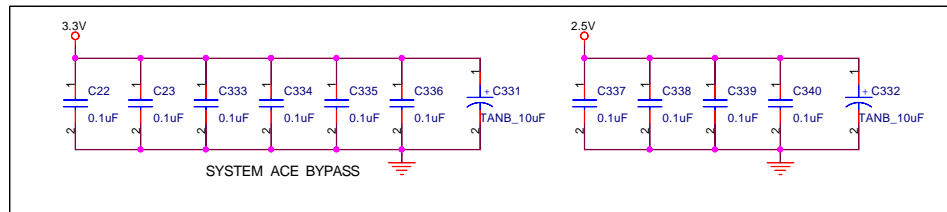
3.13.20 D[0:31] >>
 3.13.20 A[0:23] >>



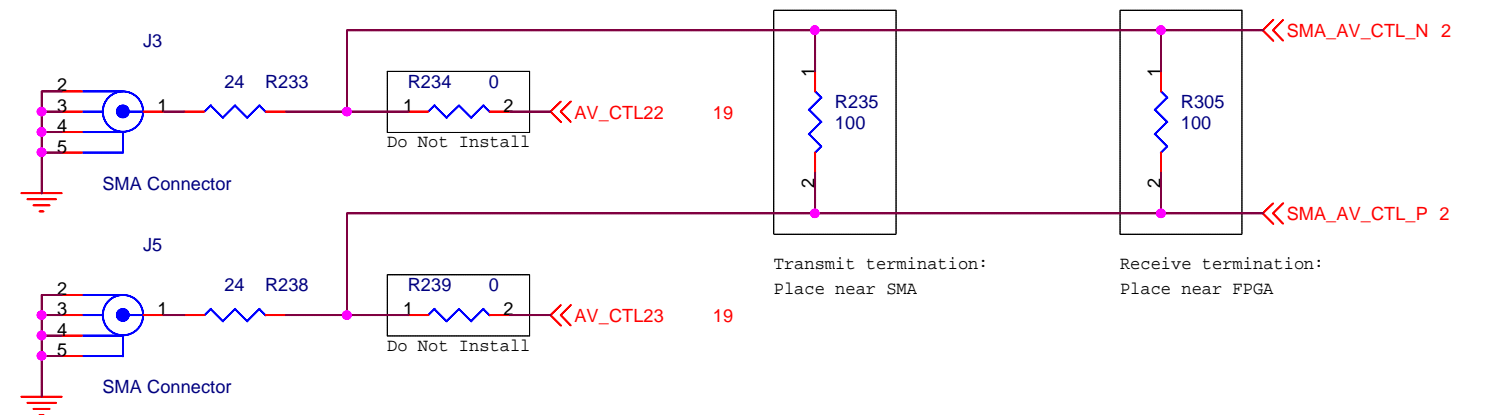
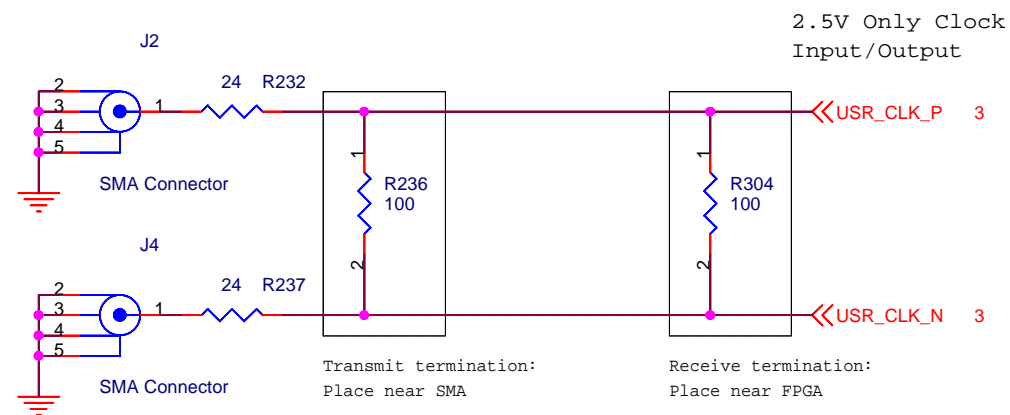
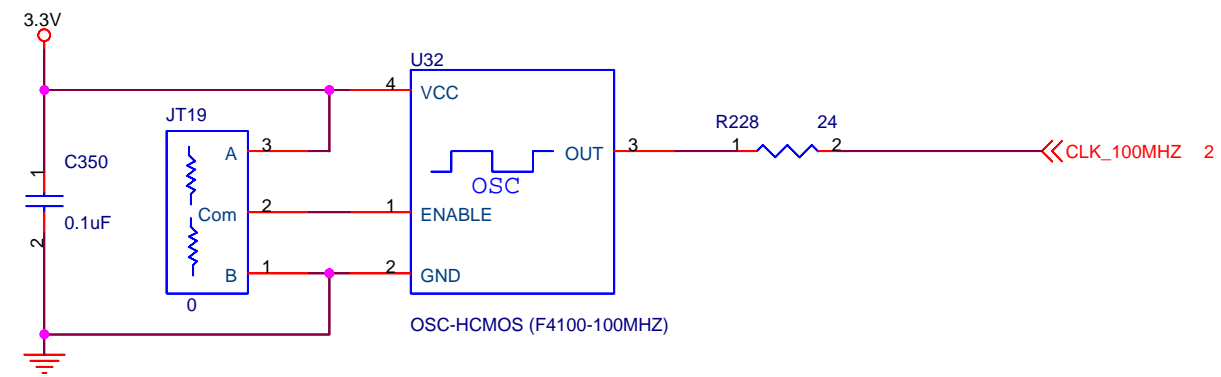
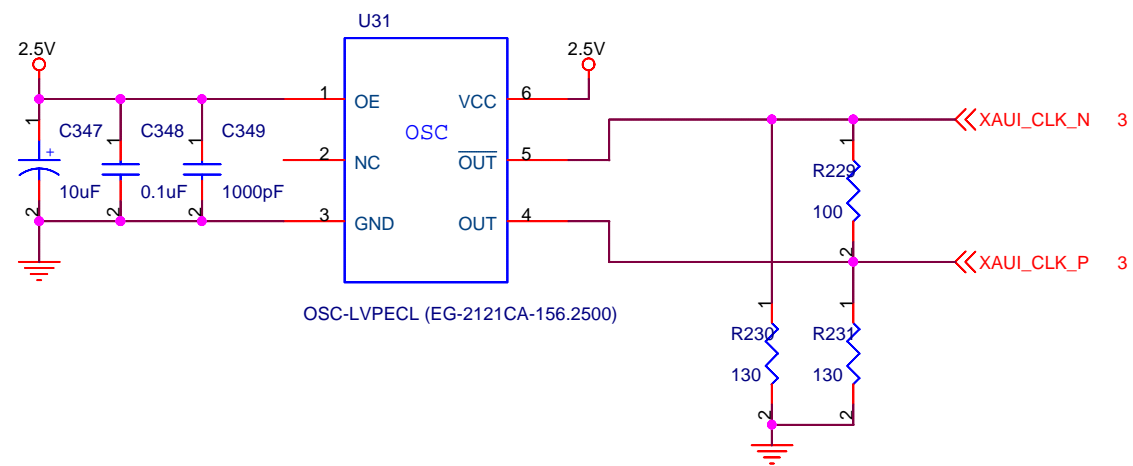
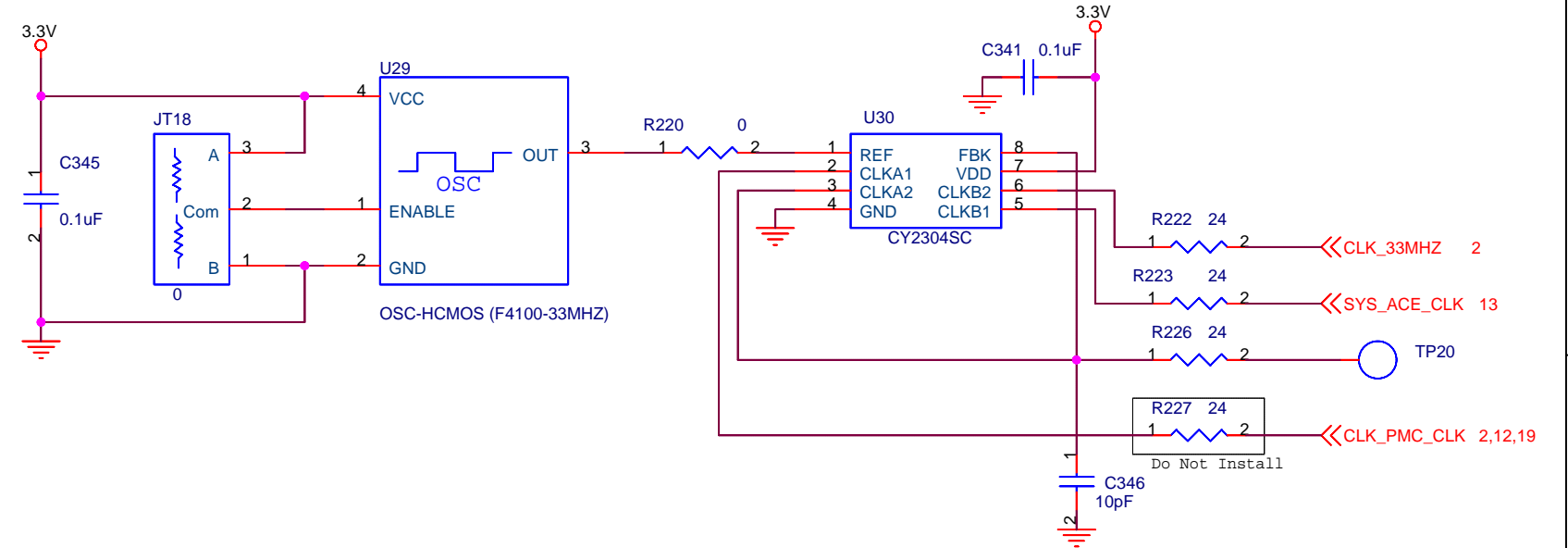
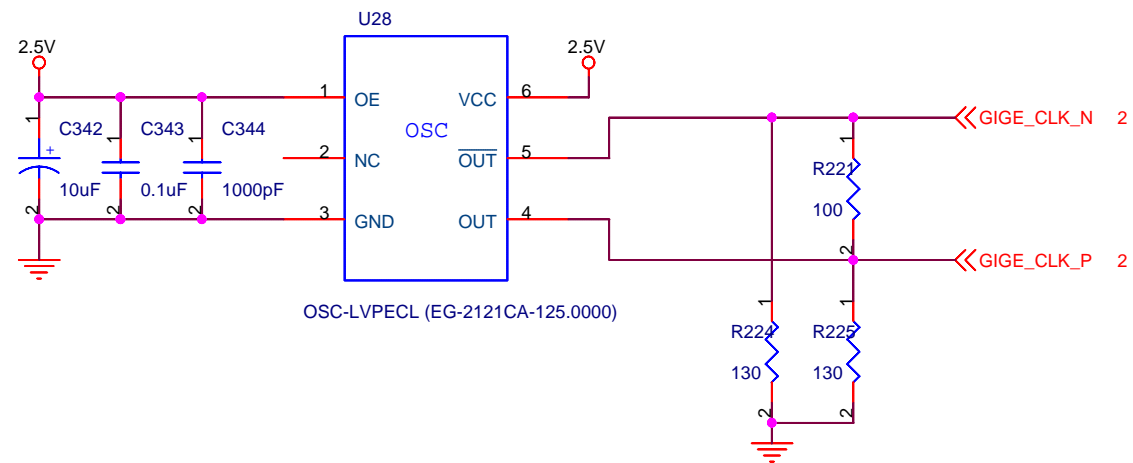
* Use SDRAM with 2.5V I/O (Mobile SDRAM)



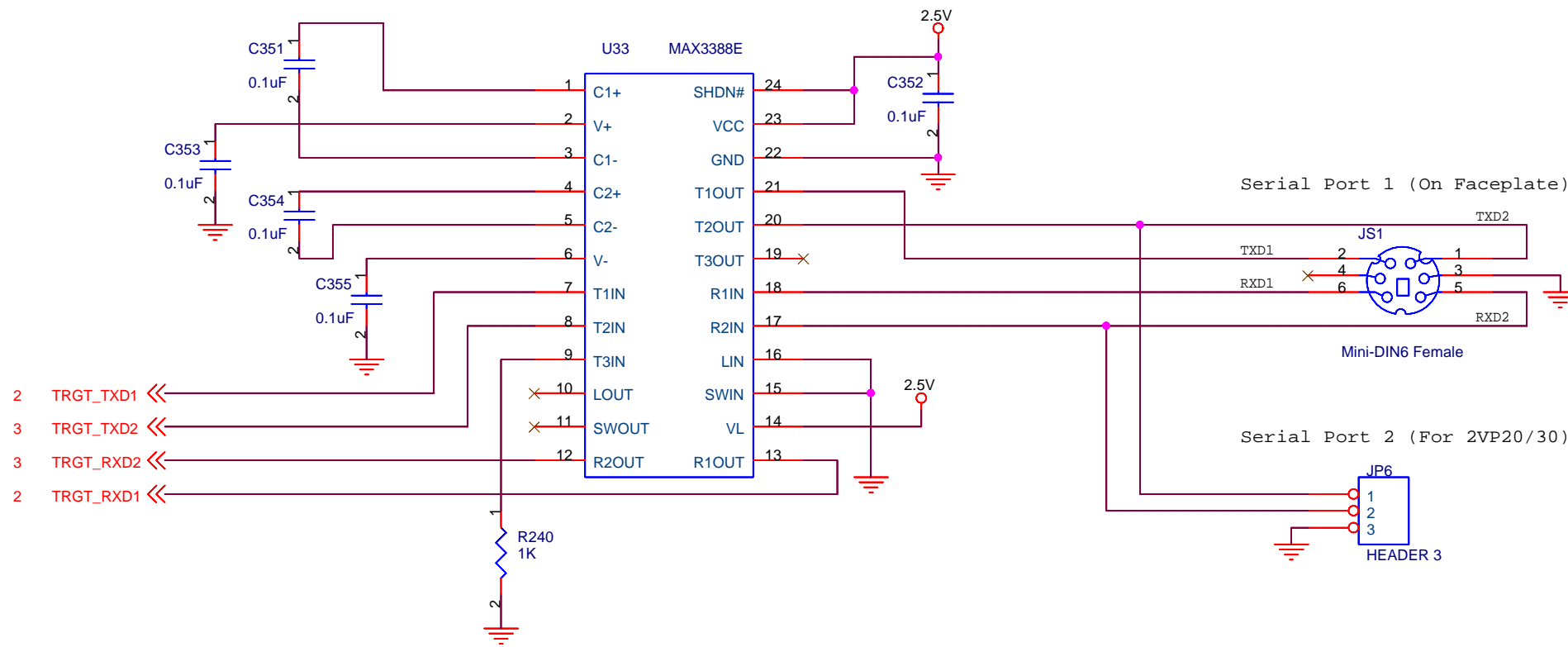
Title		
Mobile SDRAM - Target		
Size	Document Number	Rev
C	H294-XX-V2P-1103-C	C
Date:	Monday, November 03, 2003	Sheet 14 of 28



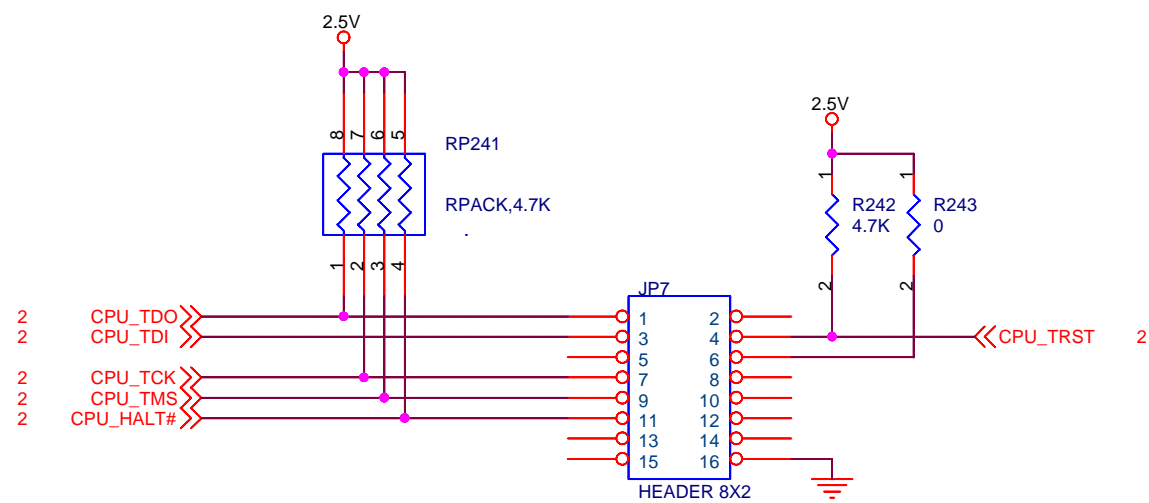
Title		
System ACE CompactFlash		
Size	Document Number	Rev
C	H294-XLX-V2P-1103-C	C
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Title Target Oscillators		
Size B	Document Number H294-XLX-V2P-1103-C	Rev C
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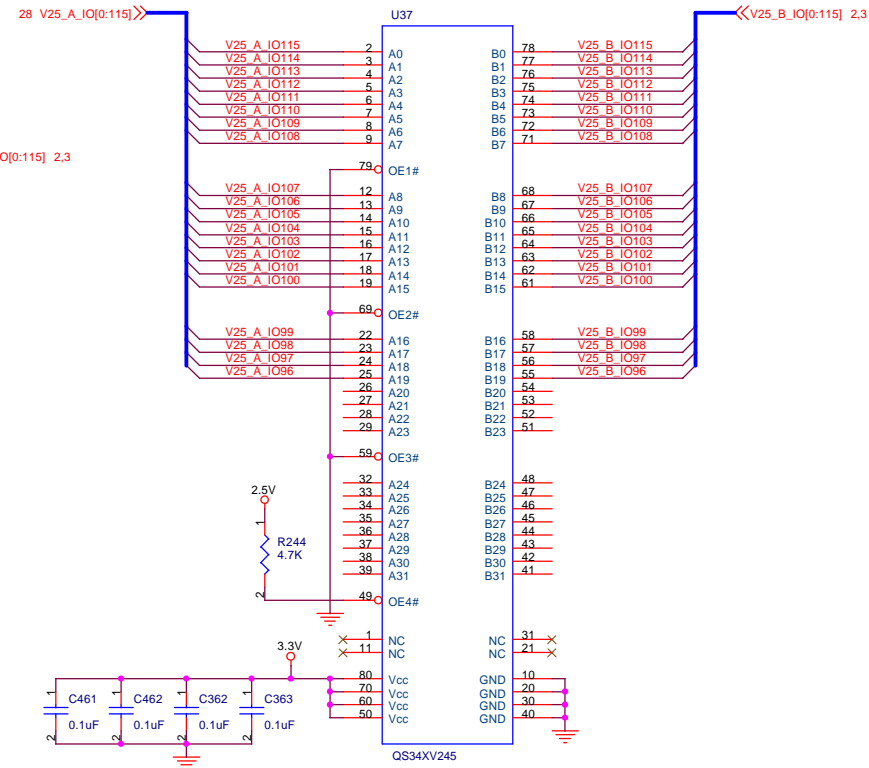
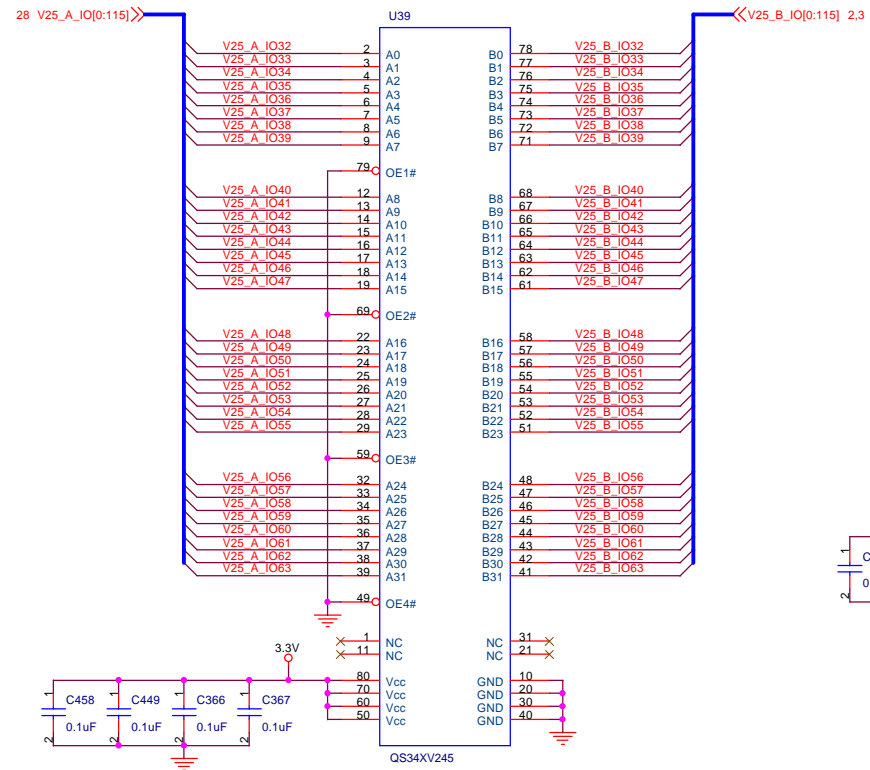
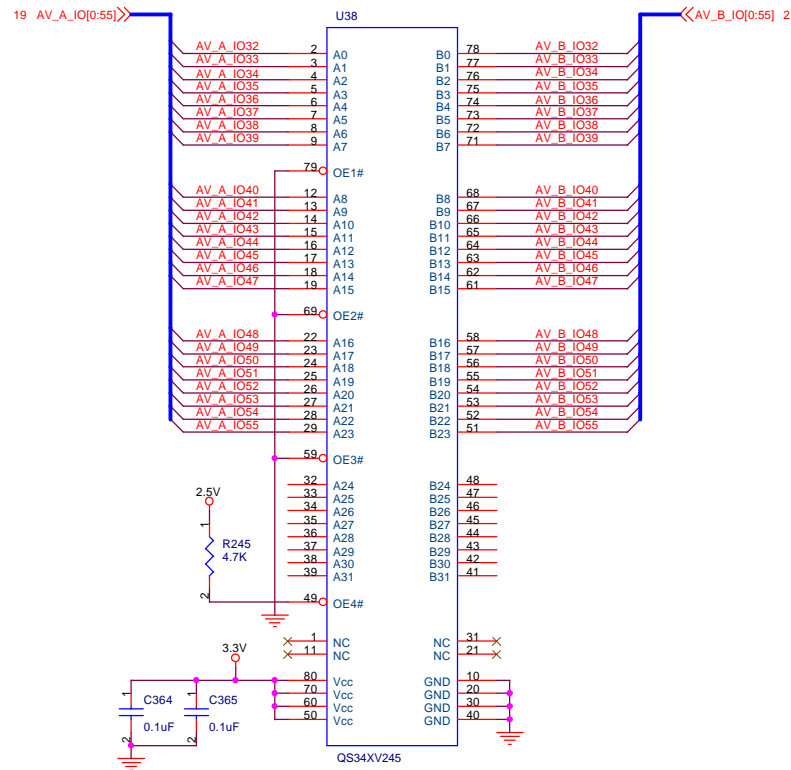
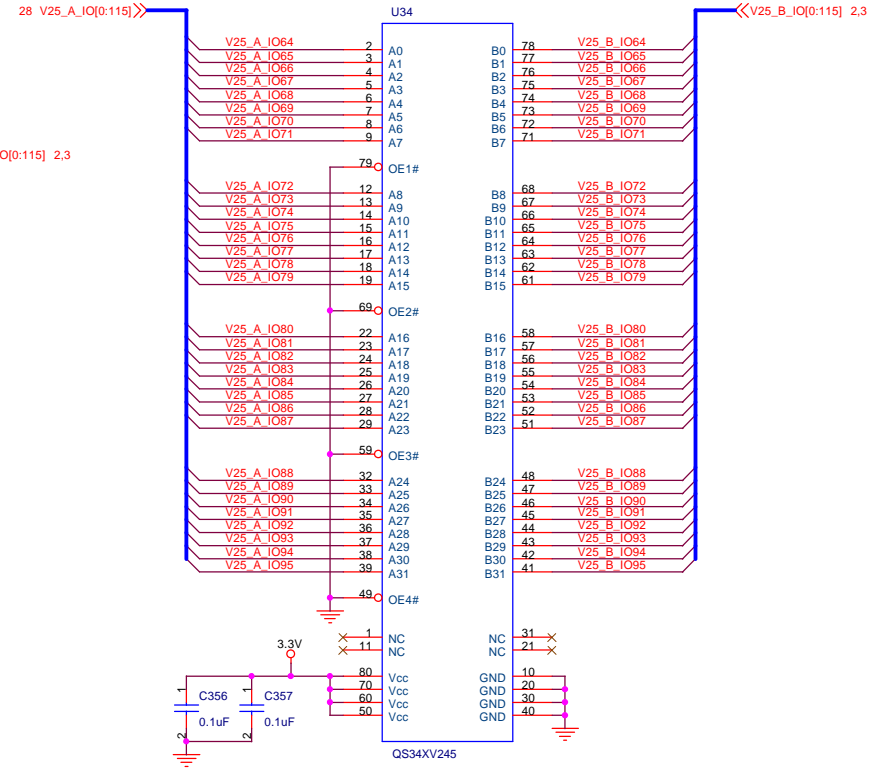
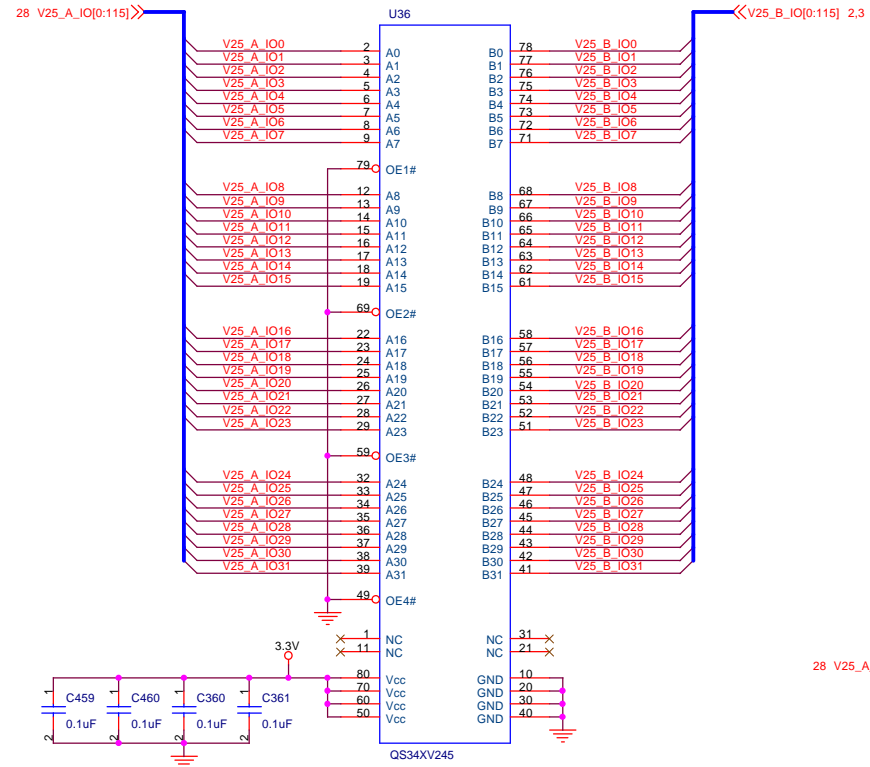
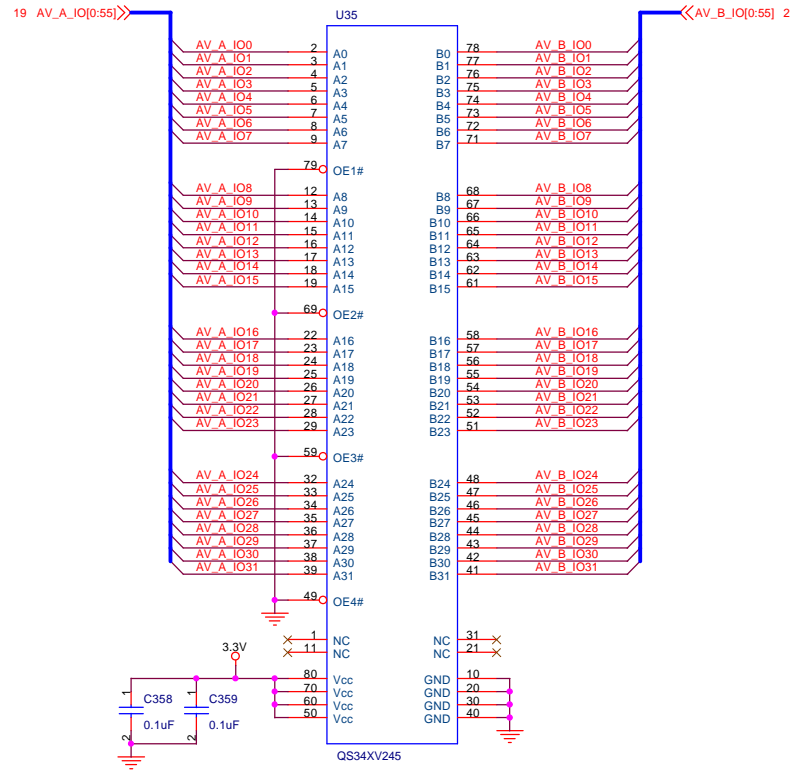
TXD2 and RXD2 can be used for flow control (CTS and RTS) for serial port 1 or for a second serial port.

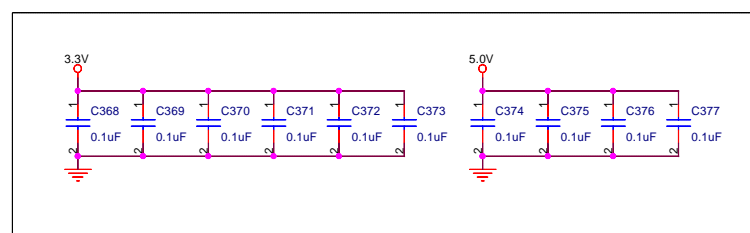
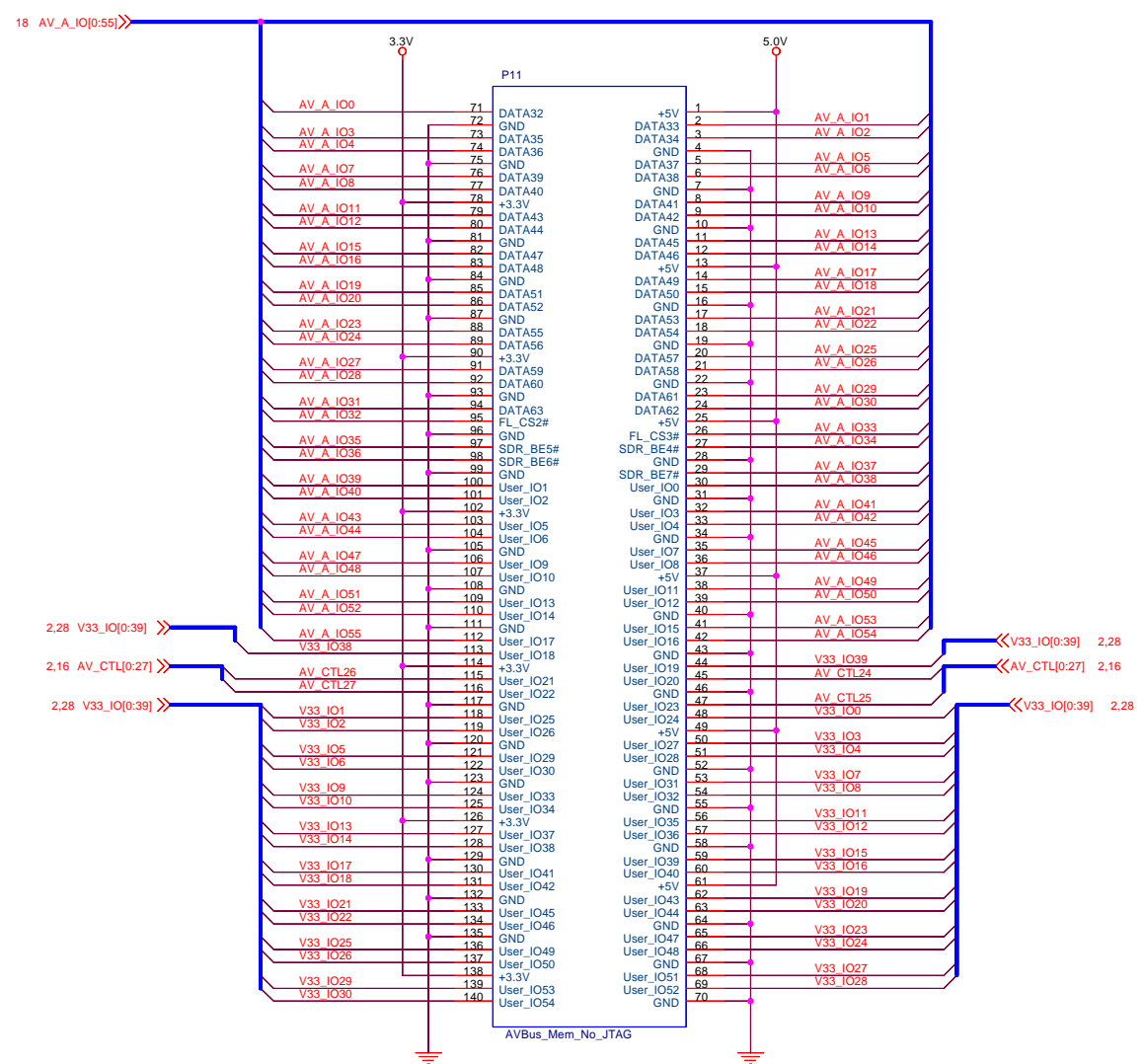
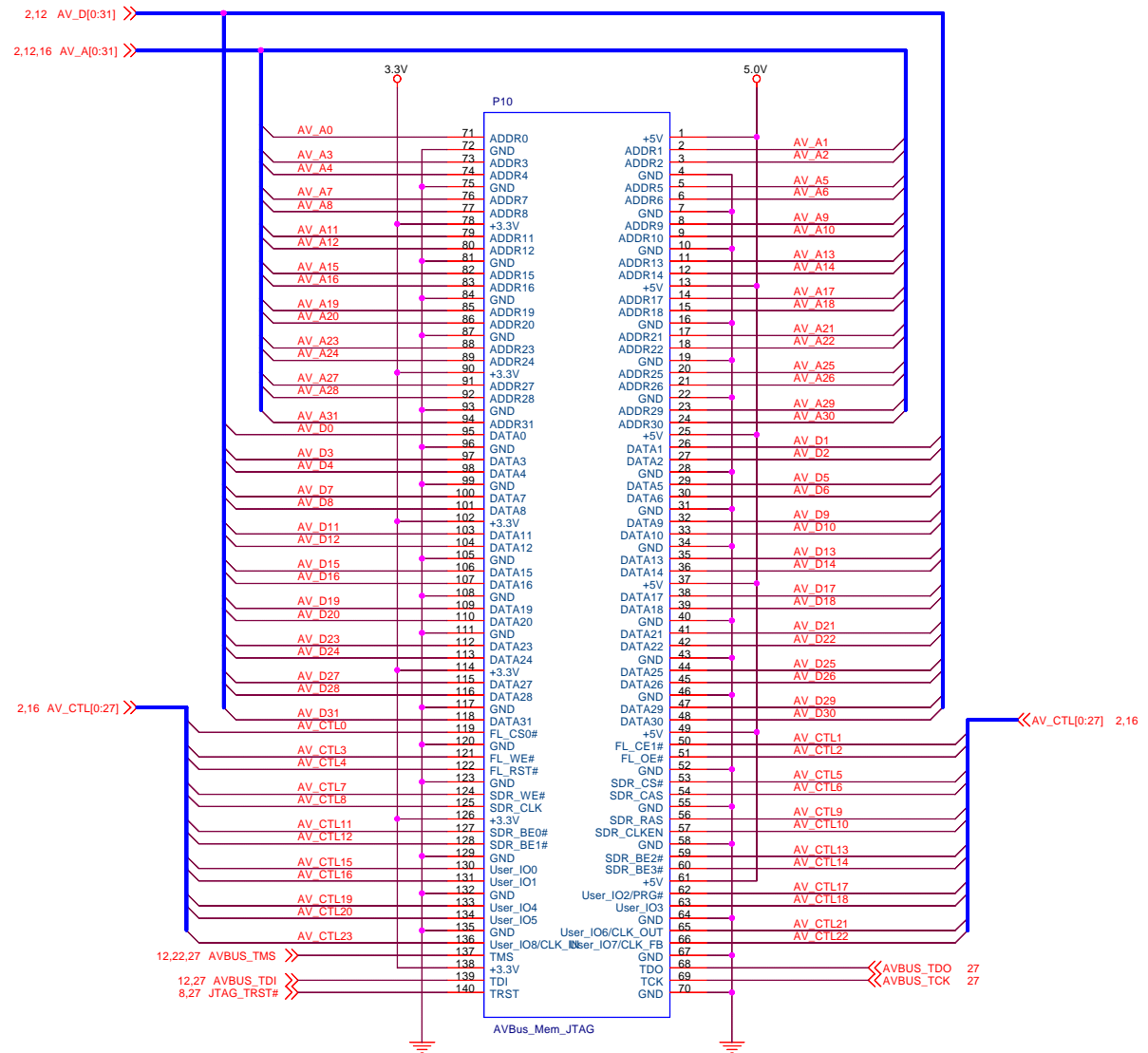


Title		
Target Debug Console		
Size	Document Number	Rev
B	H294-XLX-V2P-1103-C	C
Date:	Monday, November 03, 2003	Sheet 17 of 28

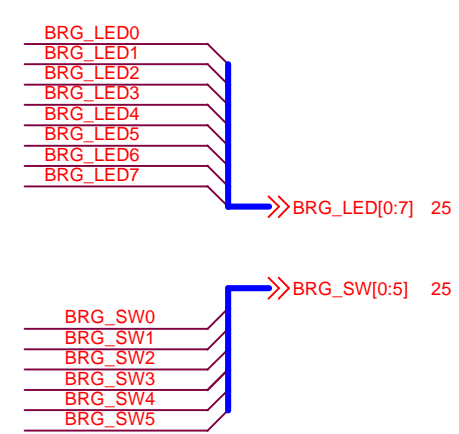
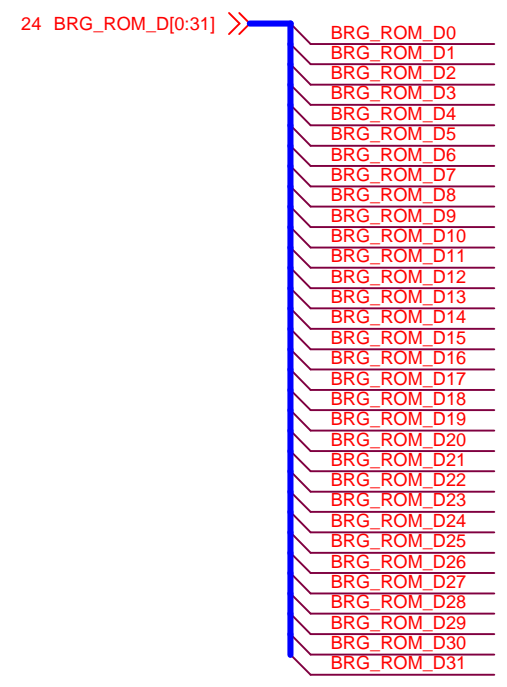
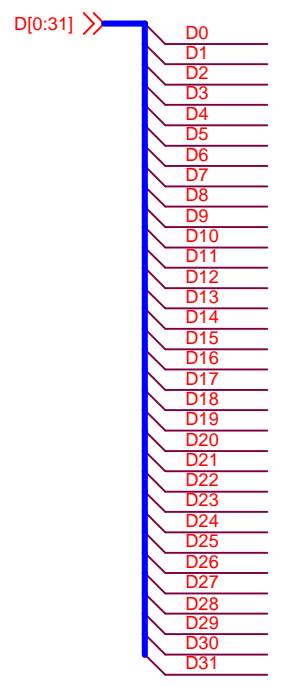
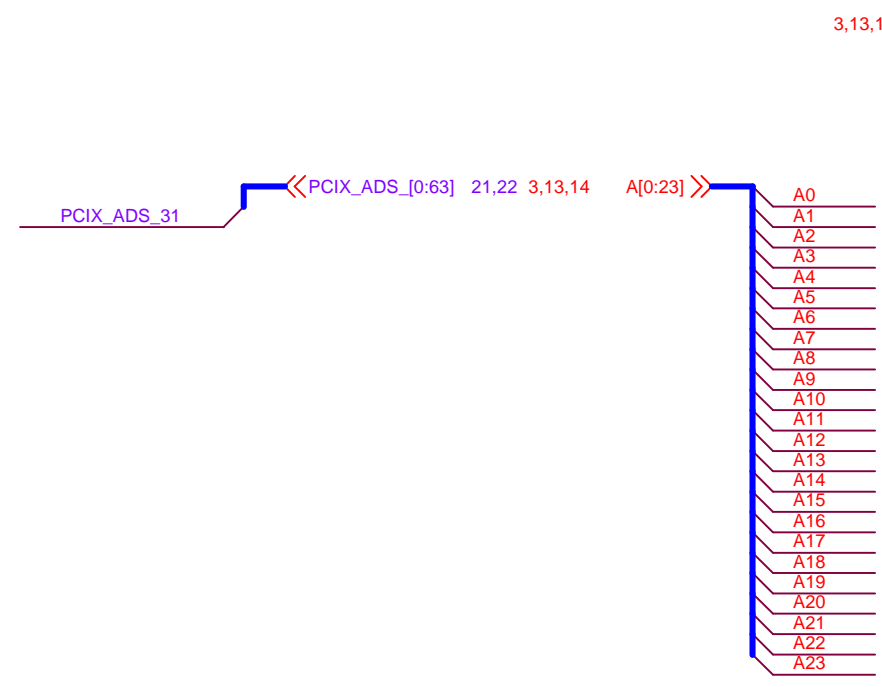
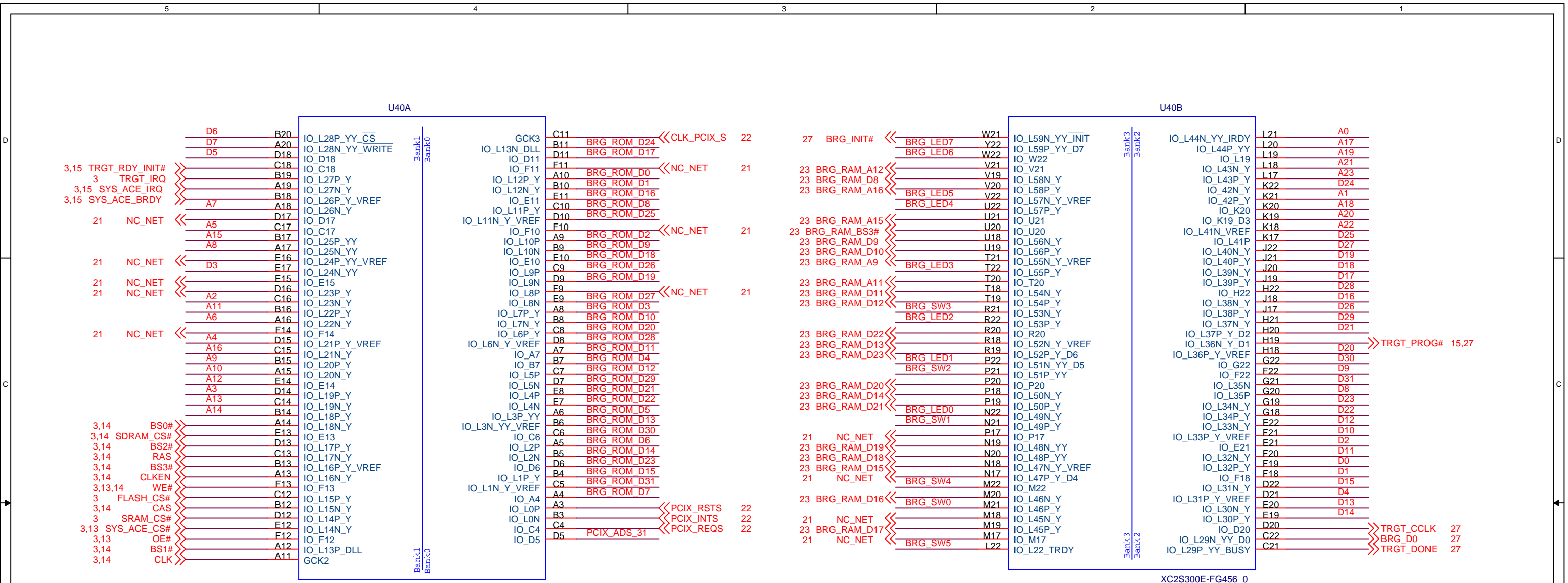
AvBus Side - 3.3V

Virtex-II Pro Side - 2.5V

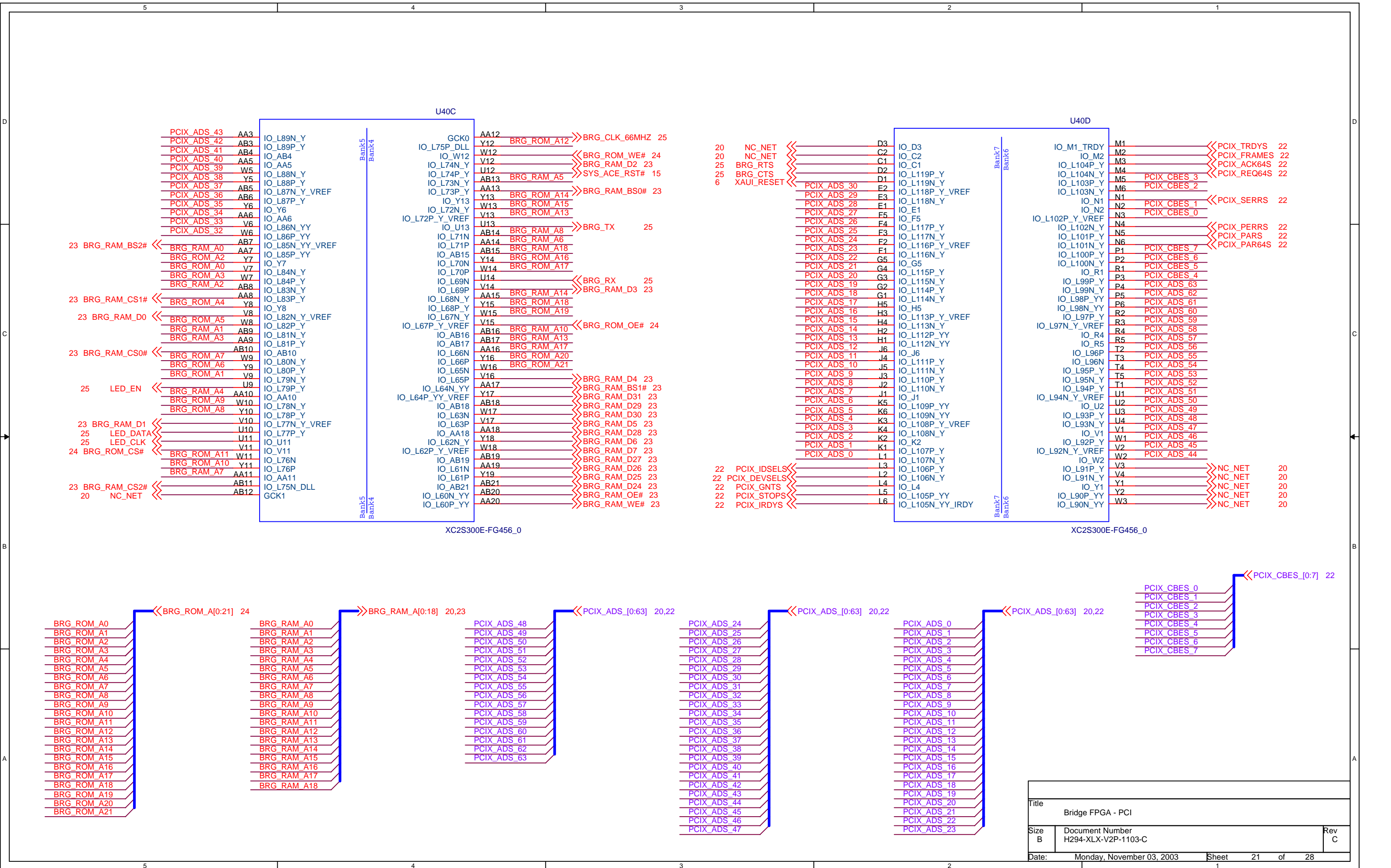




Title		
AvBus Connectors		
Size	Document Number	Rev
C	H294-XX-V2P-1103-C	C
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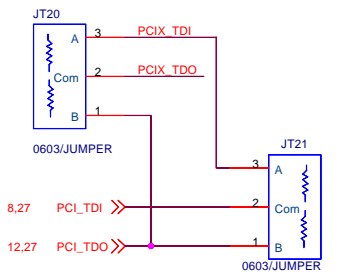


Title		
Bridge FPGA - Flash / SRAM		
Size	Document Number	Rev
B	H294-XLX-V2P-1103-C	C
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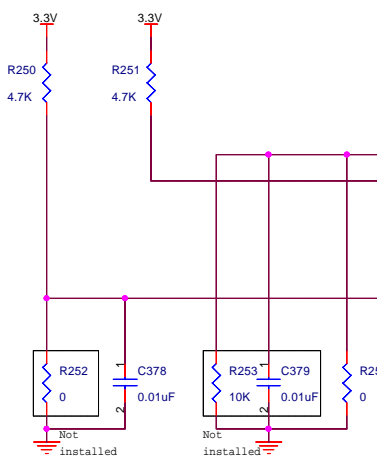
Title		
Bridge FPGA - PCI		
Size	Document Number	Rev
B	H294-XLX-V2P-1103-C	C
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NOTE: PCI CONNECTOR CONFIGURED AS 64-BIT UNIVERSAL



PCI JTAG:

JT20	JT21	Mode
1-2	2-3	PCI in System JTAG Chain
2-3	1-2	Bypass PCI JTAG

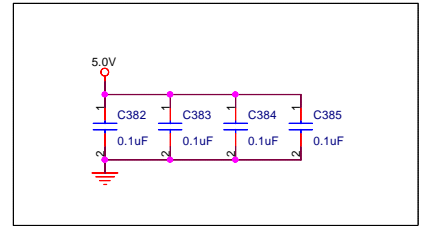
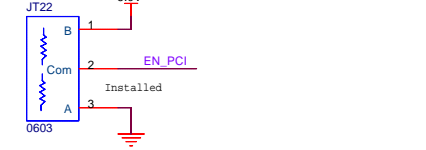
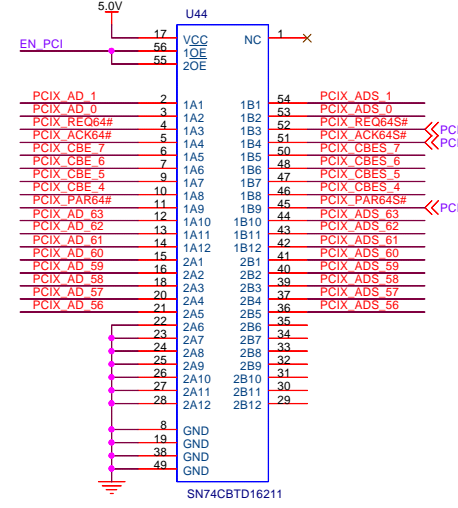
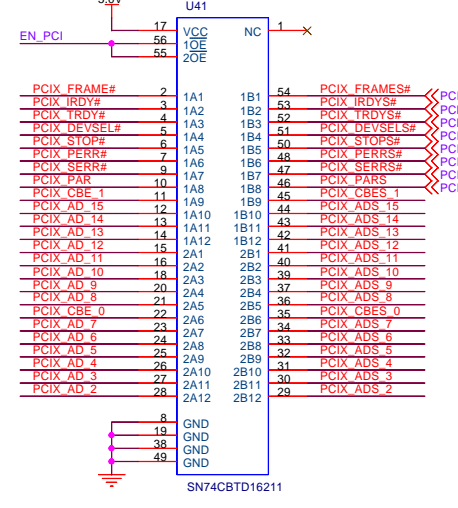
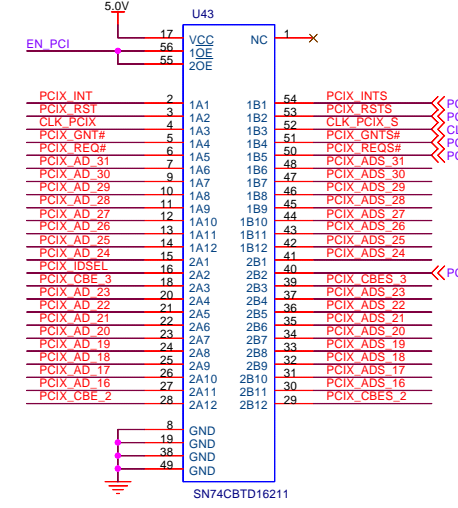
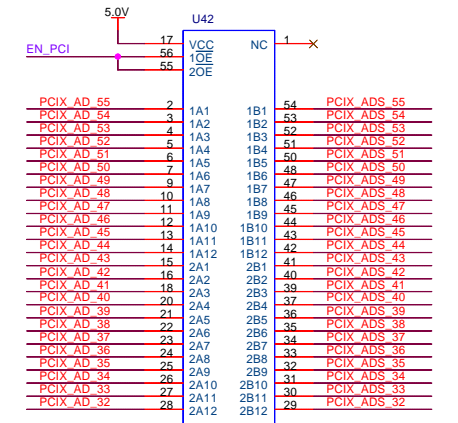
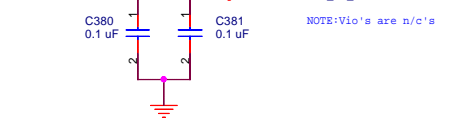
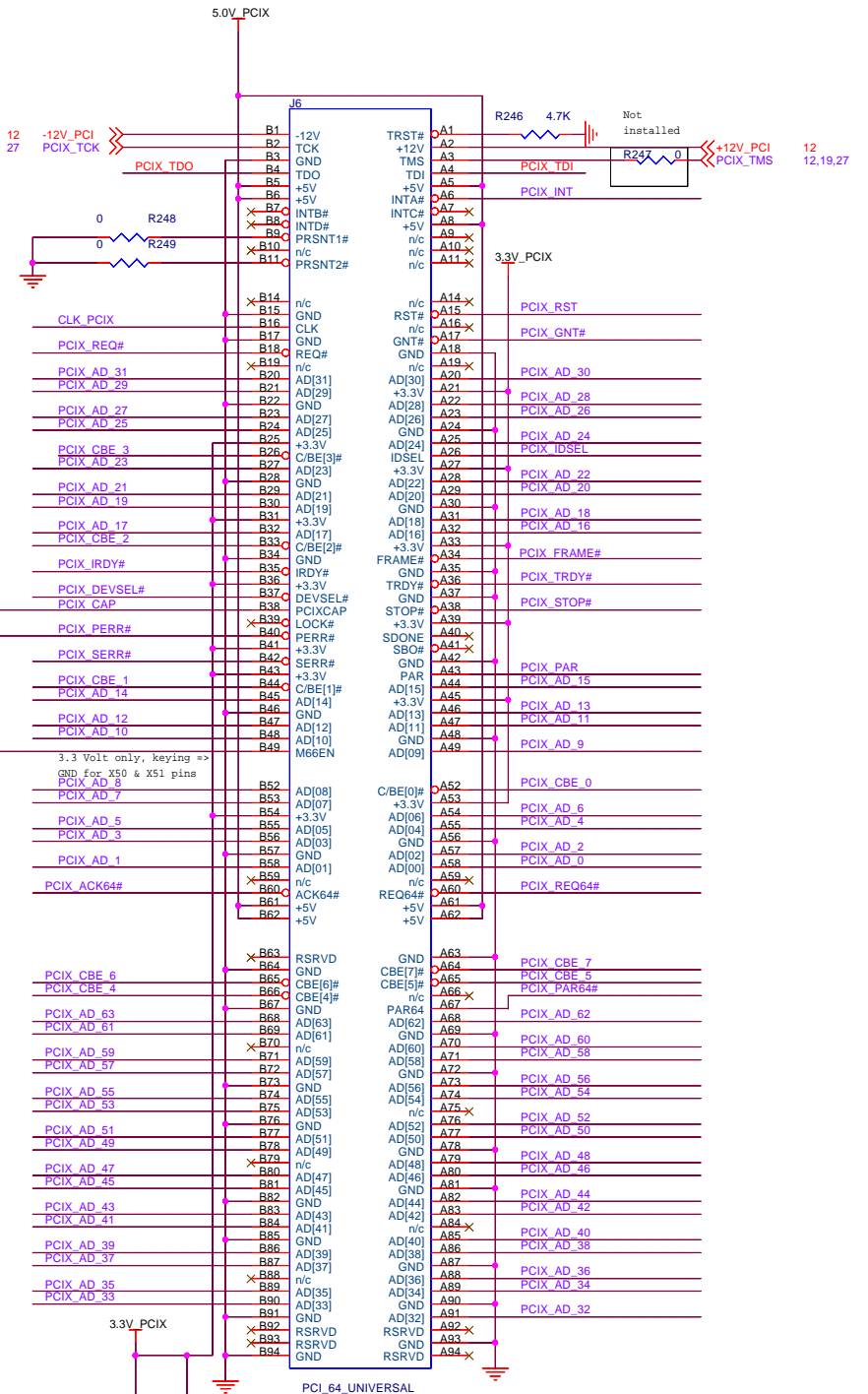


PCI CAP SIGNAL

Install R184 for PCI-X: 66MHz

Install C26 for PCI-X: 66MHz & 100MHz

Install R185 for conventional PCI



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PCI Edge Connector		
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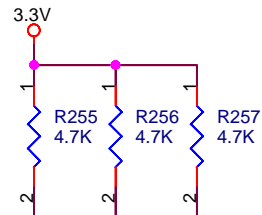
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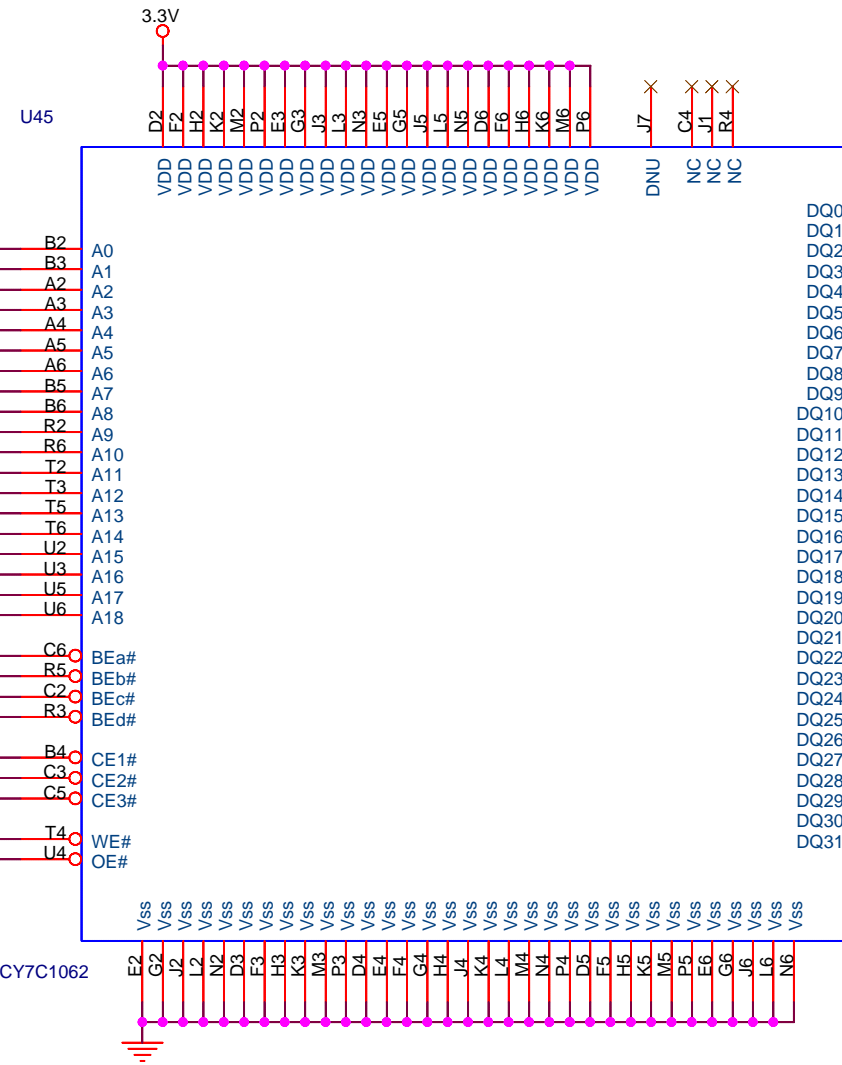
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21 BRG_RAM_BS1#
21 BRG_RAM_BS2#
20 BRG_RAM_BS3#

21 BRG_RAM_CS0#
21 BRG_RAM_CS1#
21 BRG_RAM_CS2#

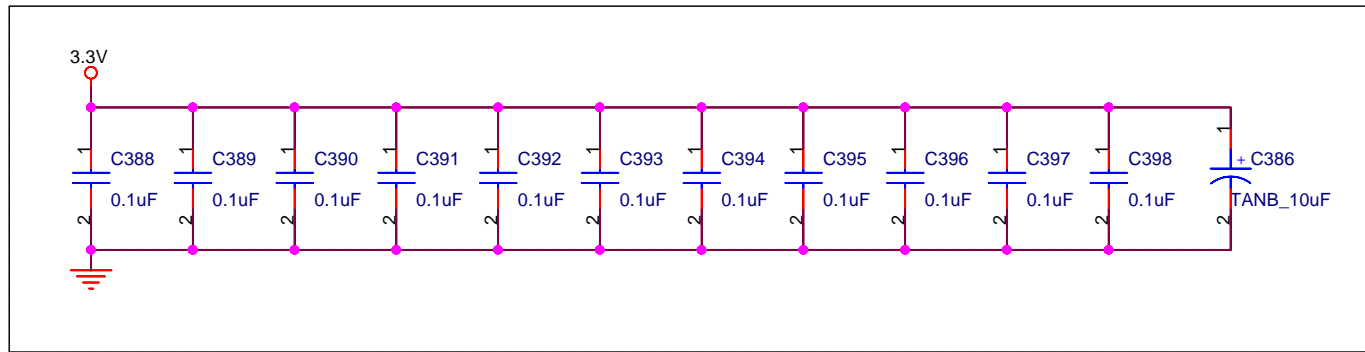
21 BRG_RAM_WE#
21 BRG_RAM_OE#



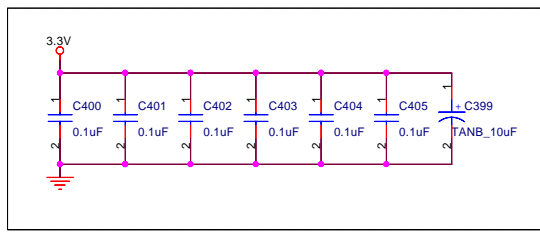
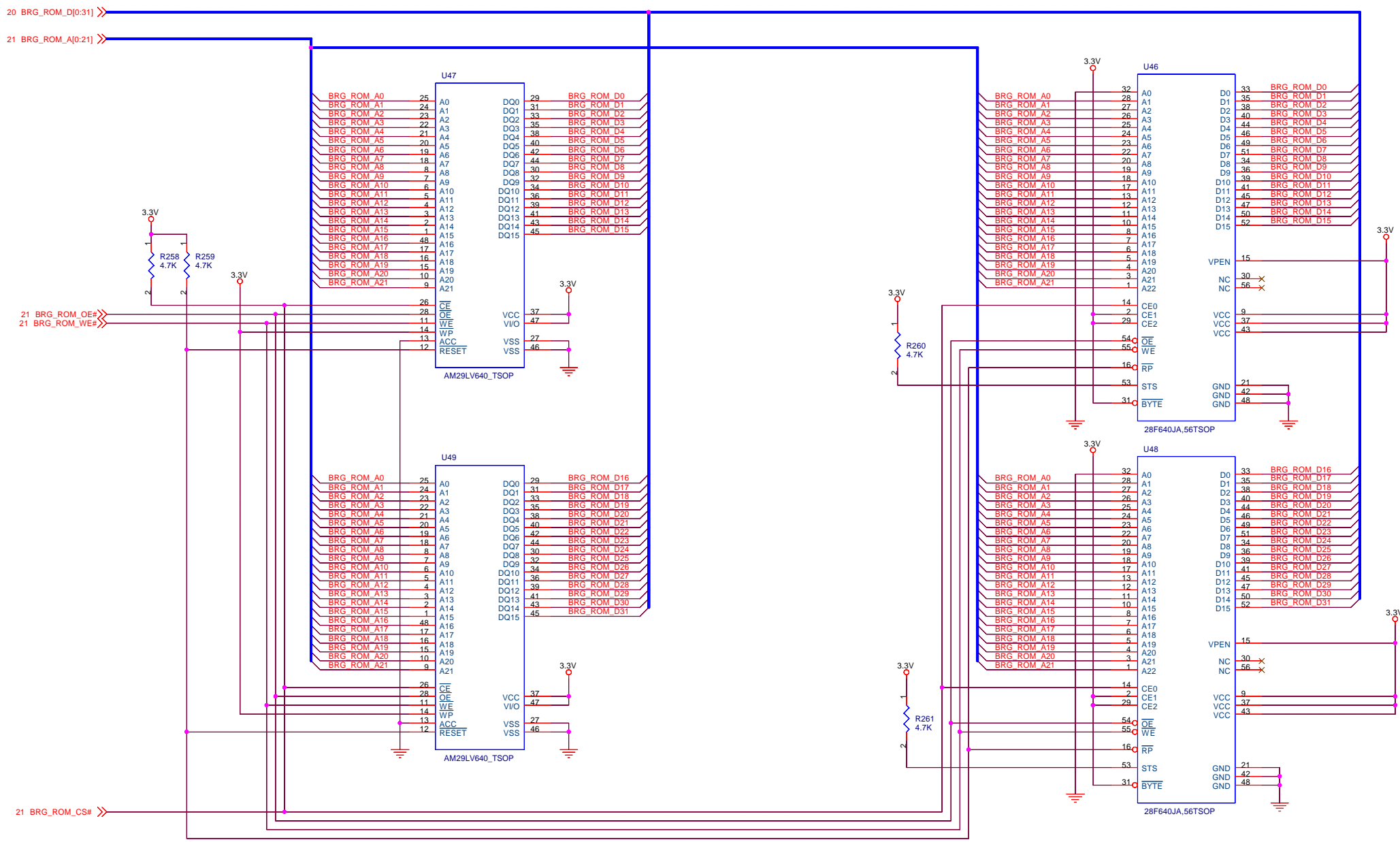
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BRG RAM A2
BRG RAM A3
BRG RAM A4
BRG RAM A5
BRG RAM A6
BRG RAM A7
BRG RAM A8
BRG RAM A9
BRG RAM A10
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BRG RAM A15
BRG RAM A16
BRG RAM A17
BRG RAM A18



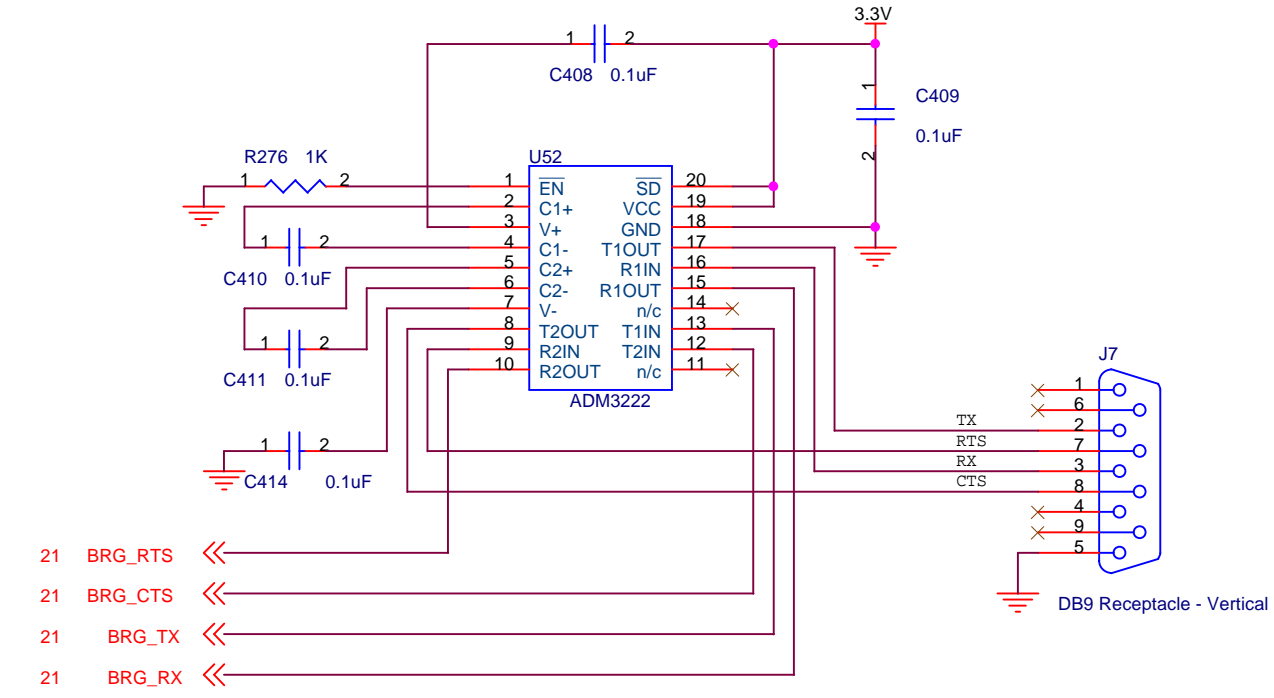
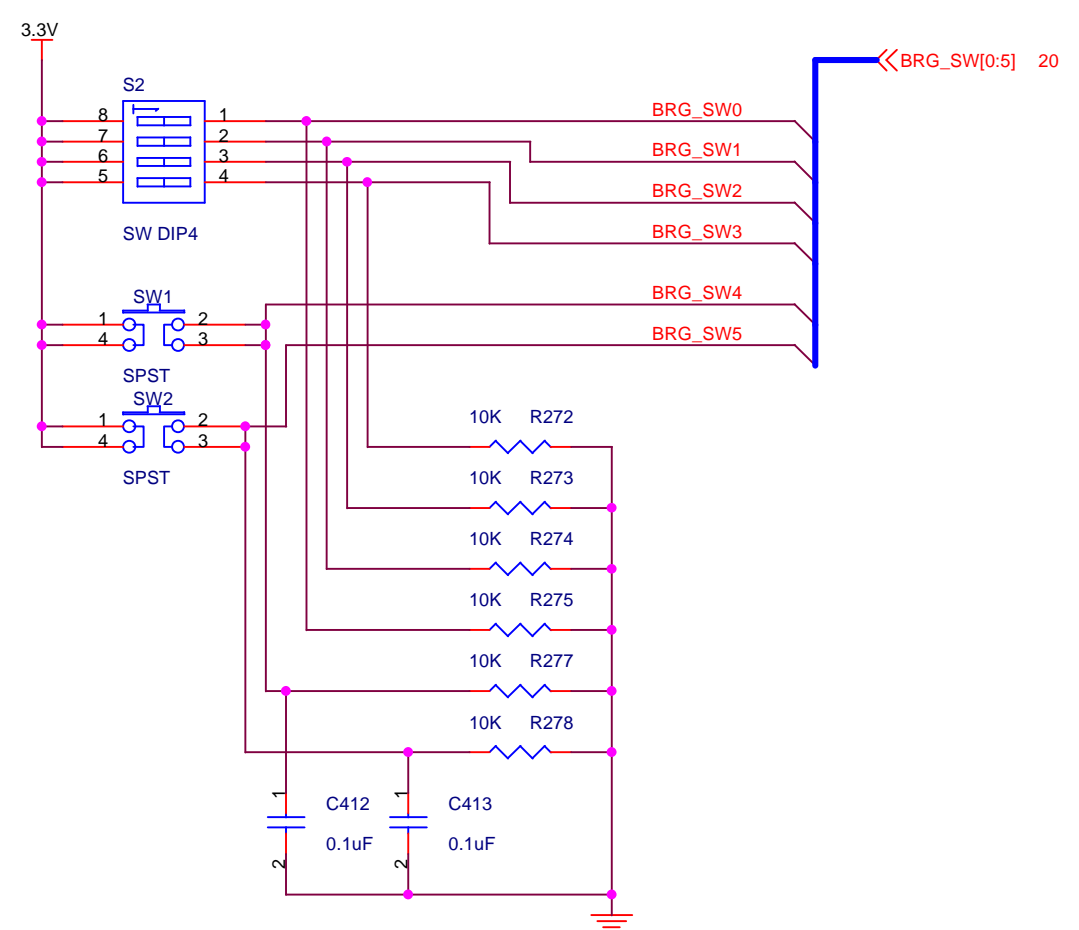
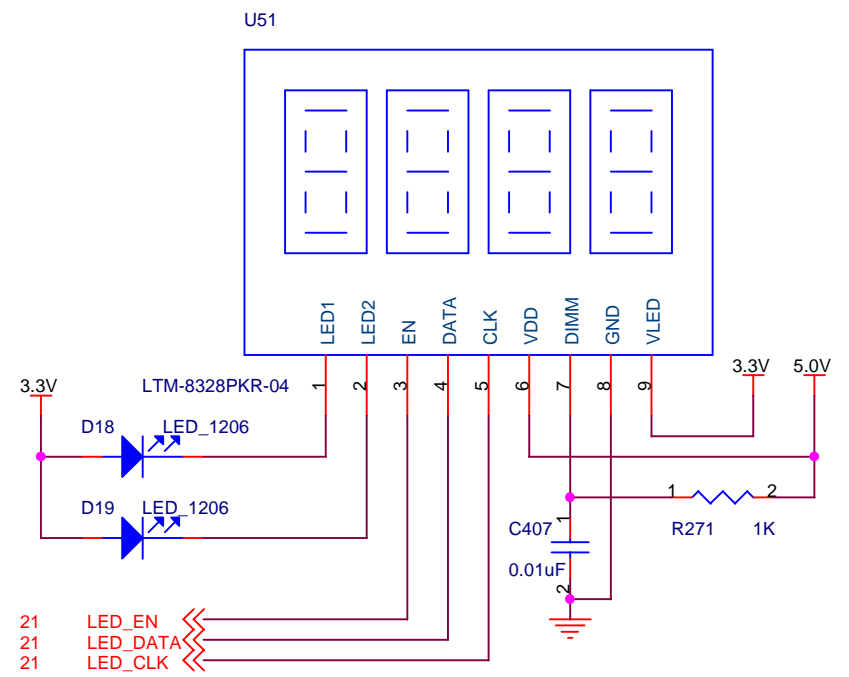
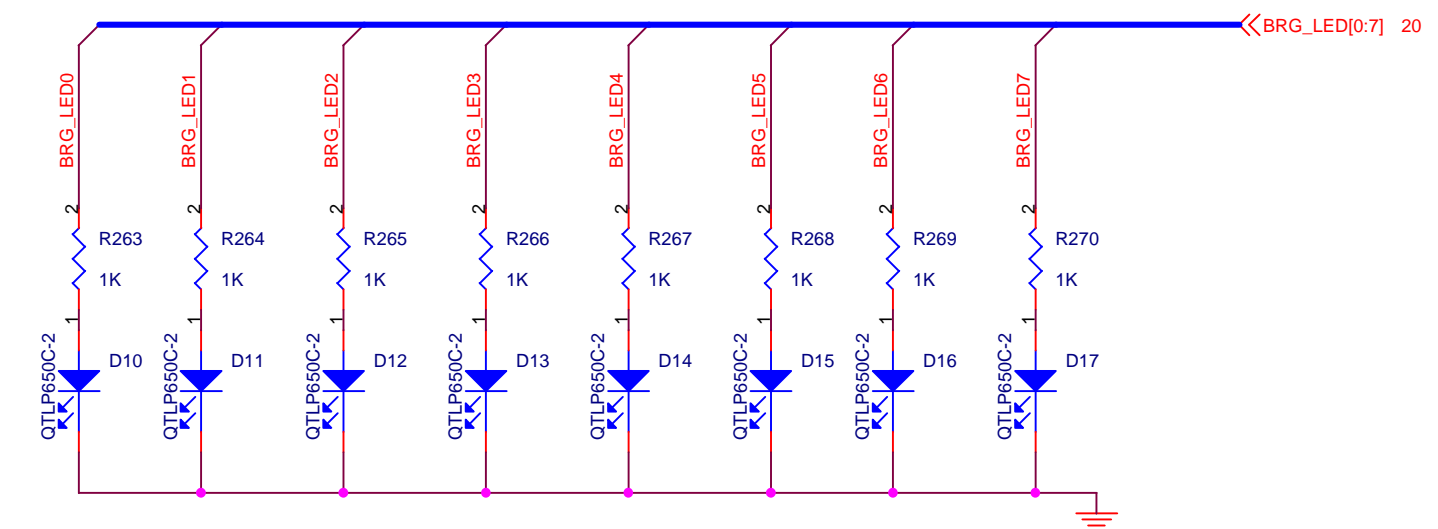
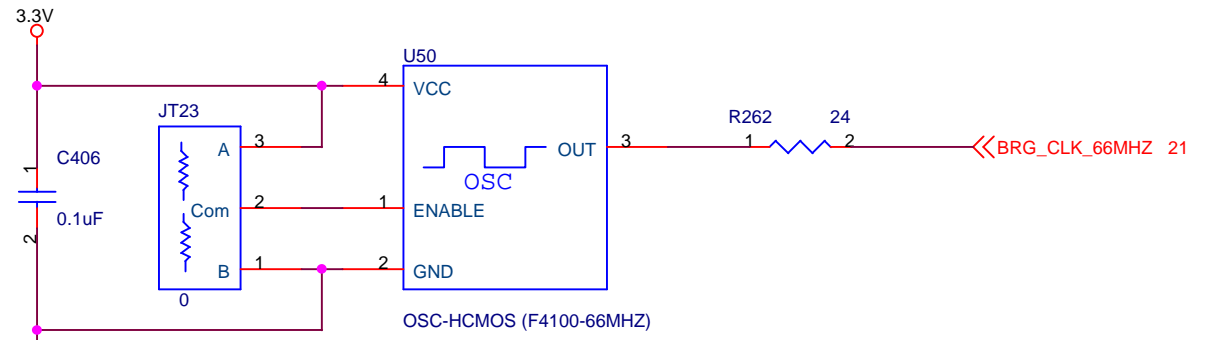
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DQ1 B7 BRG_RAM_D1
DQ2 C7 BRG_RAM_D2
DQ3 D7 BRG_RAM_D3
DQ4 E7 BRG_RAM_D4
DQ5 F7 BRG_RAM_D5
DQ6 G7 BRG_RAM_D6
DQ7 H7 BRG_RAM_D7
DQ8 K7 BRG_RAM_D8
DQ9 L7 BRG_RAM_D9
DQ10 M7 BRG_RAM_D10
DQ11 N7 BRG_RAM_D11
DQ12 P7 BRG_RAM_D12
DQ13 R7 BRG_RAM_D13
DQ14 T7 BRG_RAM_D14
DQ15 U7 BRG_RAM_D15
DQ16 A1 BRG_RAM_D16
DQ17 B1 BRG_RAM_D17
DQ18 C1 BRG_RAM_D18
DQ19 D1 BRG_RAM_D19
DQ20 E1 BRG_RAM_D20
DQ21 F1 BRG_RAM_D21
DQ22 G1 BRG_RAM_D22
DQ23 H1 BRG_RAM_D23
DQ24 K1 BRG_RAM_D24
DQ25 L1 BRG_RAM_D25
DQ26 M1 BRG_RAM_D26
DQ27 N1 BRG_RAM_D27
DQ28 P1 BRG_RAM_D28
DQ29 R1 BRG_RAM_D29
DQ30 T1 BRG_RAM_D30
DQ31 U1 BRG_RAM_D31



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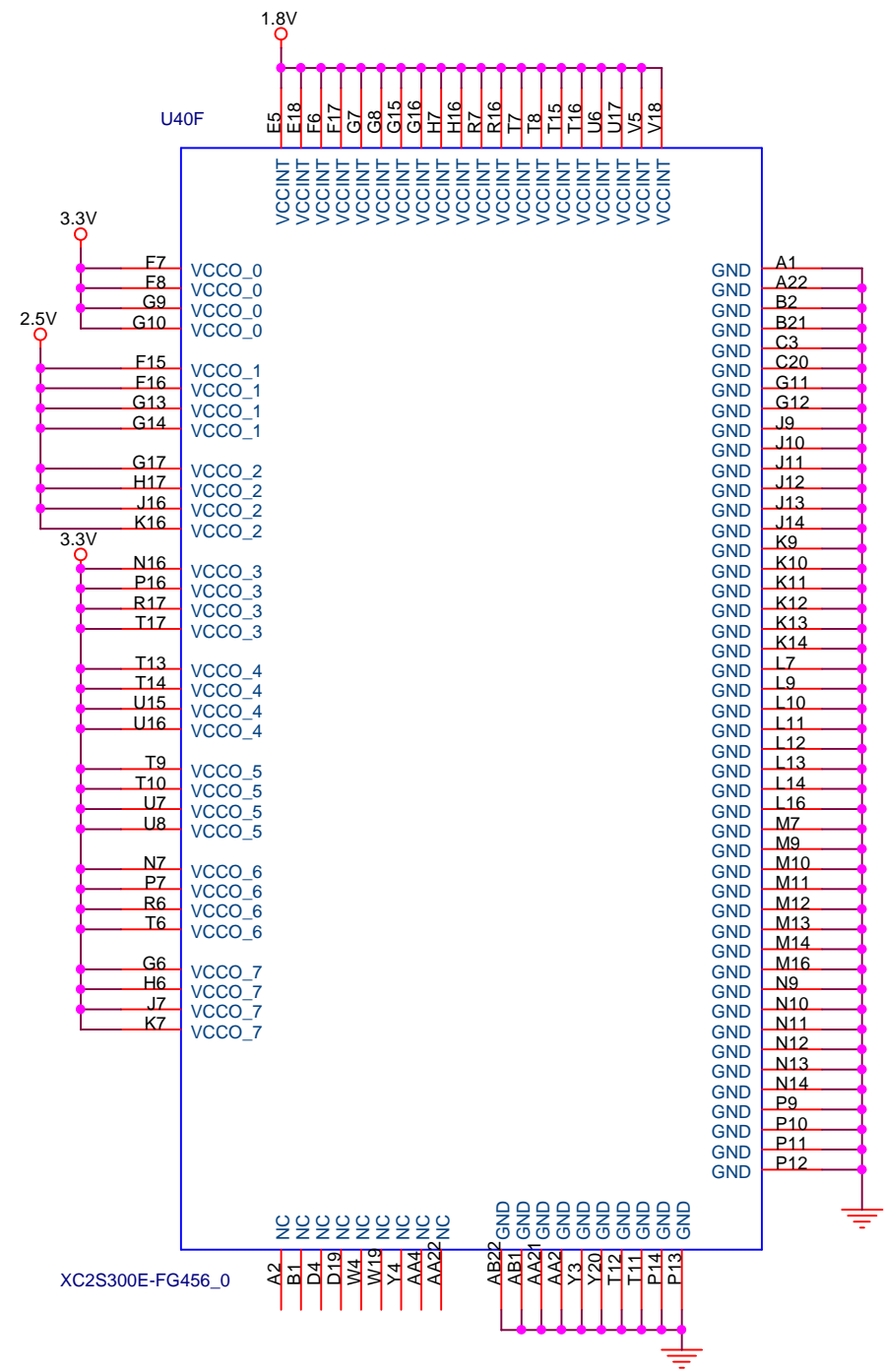
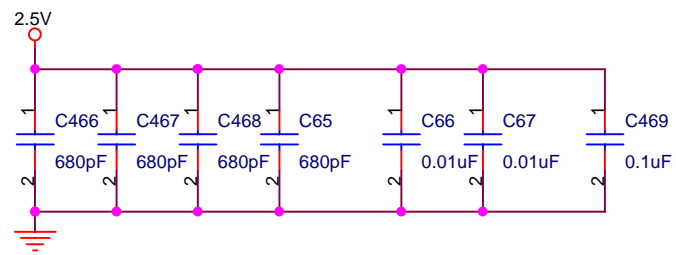
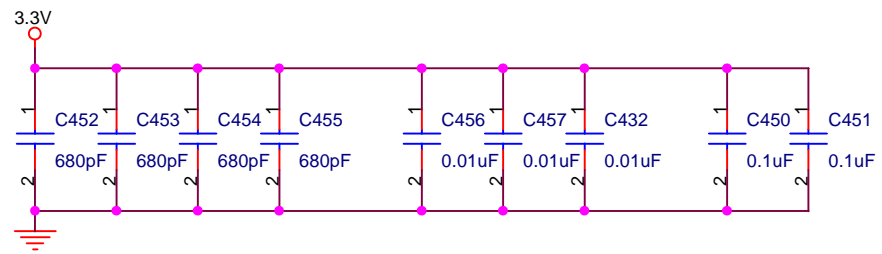
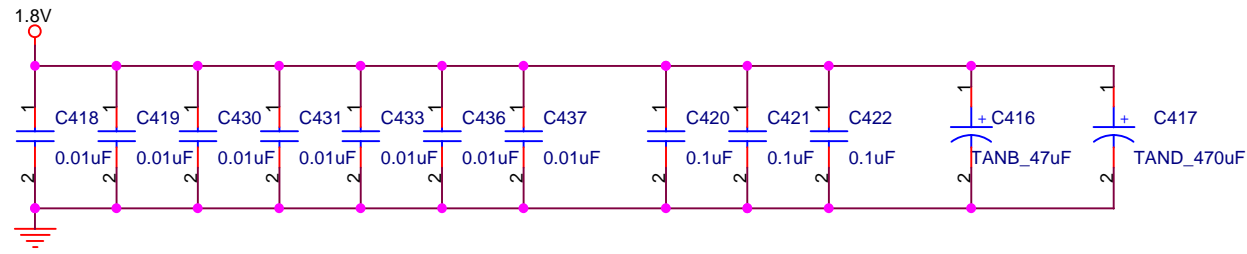


Title		
Bridge ROM		
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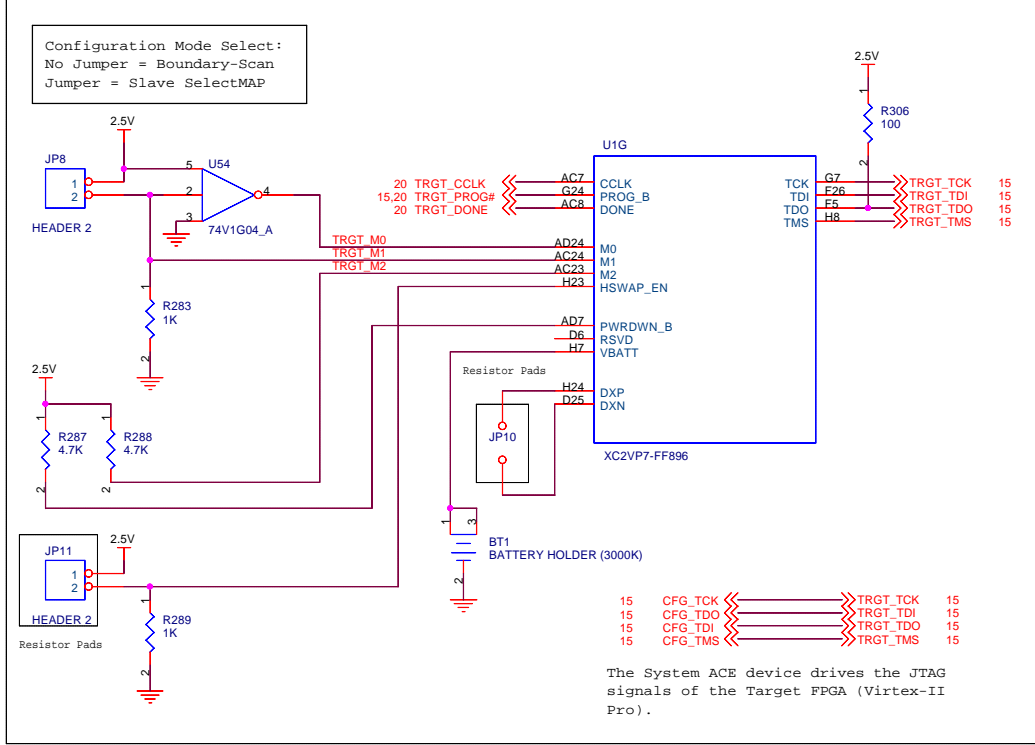
- 21 BRG_RTS <<
- 21 BRG_CTS <<
- 21 BRG_TX <<
- 21 BRG_RX <<

Title		
Bridge RS232 / LED / SW / OSC		
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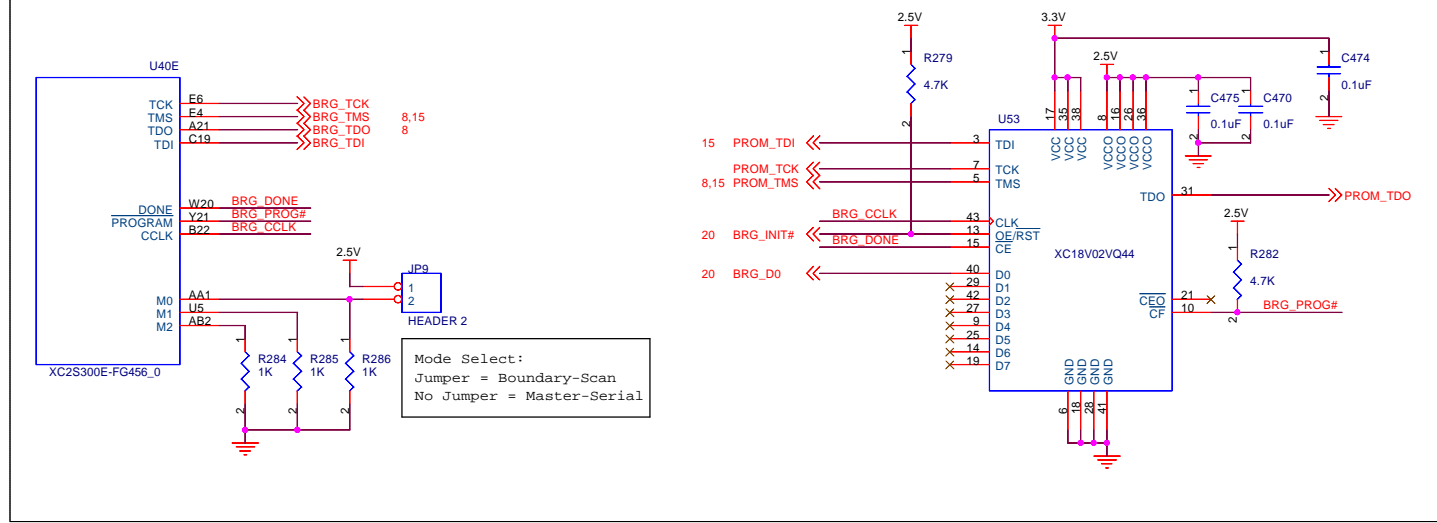


Title		
Bridge FPGA - Vcco, Vccint		
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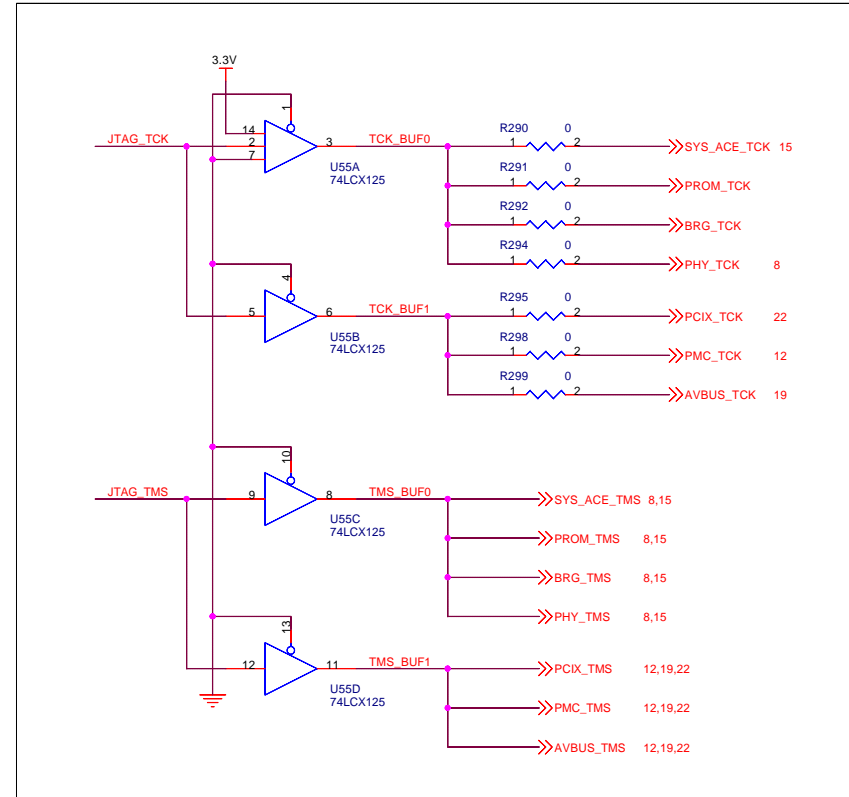
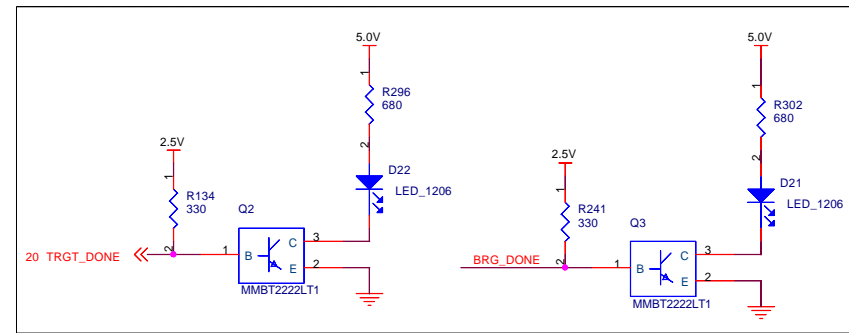
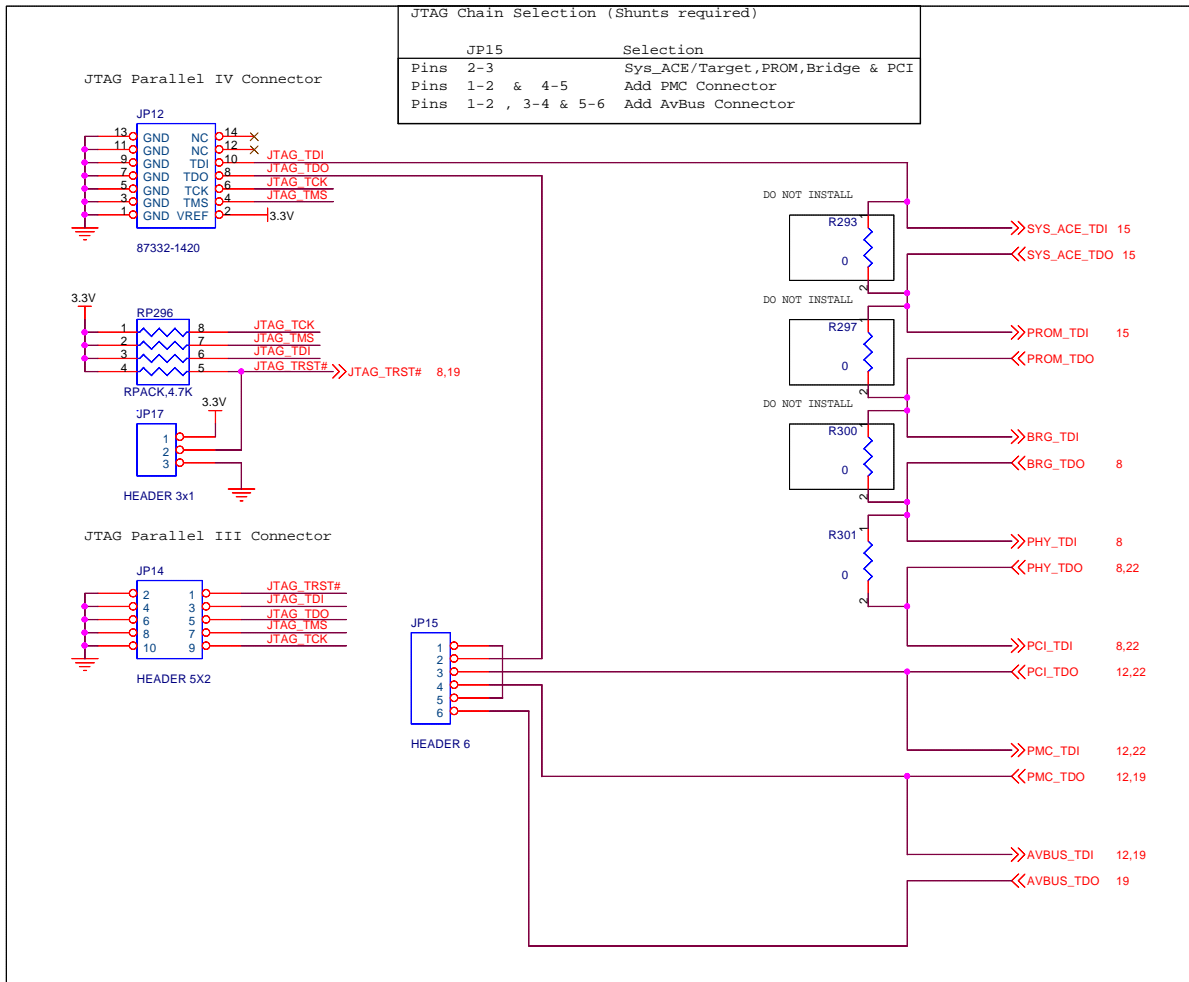
Target FPGA

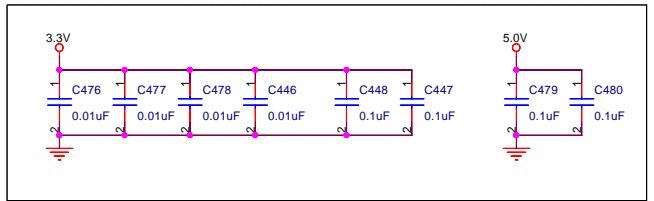
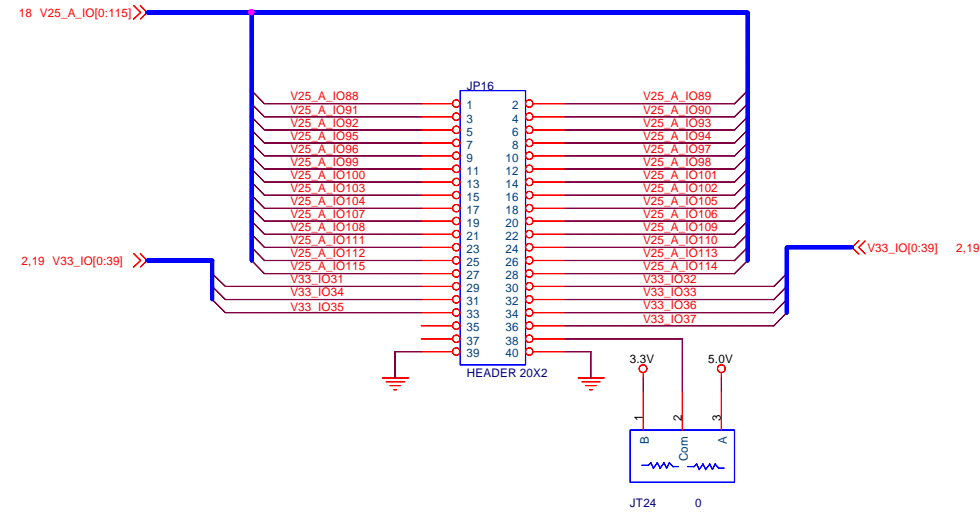


Bridge FPGA



System JTAG Connections





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AvBus - 2VP20/30 I/O		
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