

Srivatsan Parthasarathy

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About me Graduate Student at the University of Florida.

Experience **SWAMP Center** *Research Assistant*
ECE Department, University of Florida **Sep 2005 – Present**
Nanometer MOSFET modeling and Strained Silicon Measurements.
<http://www.swamp.tec.ufl.edu/>.

Tata Consultancy Services *Asst. Systems Engineer*
TCS-Motorola ODC, Madras, India **March 2004 – July 2005**
Unix Shell Scripting - Oracle PL/SQL Database management - PL/SQL programming - Developing and testing Business Intelligence Reports using Oracle Reports and Cognos Impromptu - Global Production Support for a SOX Level 1 Financial Engine - Quality Control. <http://www.tcs.com/>.

Education *Master of Science in Electrical Engineering*, (expected May 2007)
University of Florida, Gainesville, FL.

Courses: Bipolar Analog IC Design; MOS Analog IC Design; VLSI circuits and Technology; Advanced VLSI Design; Advanced Computer Architecture.

Bachelor of Engineering, May 2003
University of Madras, Chennai, India.
GPA: 3.96/4

Relevant Courses: Semiconductor Device Fundamentals; Electronic Circuit Design; Linear Integrated Circuits; Microprocessor Design and Applications; Digital Systems Design; Principles of Digital Computers; Electronic Circuits laboratory; Integrated Circuits laboratory; Microprocessor Laboratory; Digital Design laboratory.

- Publications**
1. P. Srivatsan, S. Thompson, “*The State of Moore’s Law and The Real Limiters to Sub-20nm Transistors*” (Under review).
 2. P. Srivatsan, “*A Framework for Power Efficient Instruction Encoding in Deep Sub-Micron Application Specific Processors*” (To be submitted to IEEE Application Specific Systems, Architecture and Processors (ASAP 2006))
 3. P. Srivatsan, N. Ramachandran, “*DSM interconnect Modeling using Step Response Integral Square Error Minimization*” (To be submitted)
 4. P. Srivatsan, P.B. Sudarshan, P.P. Bhaskaran, “*DYNORA: A New Caching Technique*”, 3rd IEEE EuroMicro Symposium on Digital System Design, (Euro DSD-2003), Turkey, Sep. 2003.
 5. P.B. Sudarshan, P. Srivatsan, “*Towards a Strongly Fault Tolerant VLSI Processor Array*”, 12th IEEE North Atlantic Test Workshop (NATW-2003), New York, May 2003.

- Projects**
1. Op-amp Design project, part of MOS Analog IC Design course at UF
 2. 32-bit high-speed Adder Design (parallel-prefix adder, Kogge-Stone type), part of Advanced VLSI Design Course at UF.
 3. 18-bit Synchronous SRAM Design, part of VLSI Circuits and Technology course at UF.
 4. Datapath and Control Unit Design for a 32-bit RISC Microprocessor, part of undergraduate coursework.

Skill Set

CAD Tools	Cadence, PSpice
Design Environment	MATLAB
Timing/Simulation	ModelSim, Xilinx Student Edition F1.5
Programming	C, 80x85 & 80x86 assembly, VHDL, Oracle PL/SQL
Scripting	Sed, Awk, Unix Shell Scripting (bash & ksh)
Operating Systems	Solaris, Linux, Windows 9x/XP/NT