Emerging Research Devices: A Study of CNTFET and SET as a replacement for SiMOSFET

Mahmoud Lababidi, Krishna Natarajan, Guangyu Sun

Abstract— Since the development of the Silicon MOSFET, it has been the leading technology as it gave the designer the freedom to scale, pack more devices/area along with increased performance. We are at a point that scaling MOS is no more easy. As we approach the scaling limits of MOSFETs, there lies the imposing question of will this limit be the end of MOSFET or will it be the beginning of new devices that will take over from where SiMOSFET left off. Many New Devices which have properties that make them a candidate to replace SiMOSFET are currently under study. The frontrunners being the CNTFET and SET. In comparing these devices with SiMOSFET, the operations, obstacles and challenges in designing these devices are put to light and their feasibility in replacing SiMOSFET is analysed.

I. INTRODUCTION

Silicon MOSFETs have been the dominant technology for developing analog and digital circuits for the past 2 decades or so. In these years, tremendous strides were made in terms of scaling and improving performance. As the device sizes came down, certain undesirable effects that were previously immaterial in long channel device surfaced. Though, these ill effects of device scaling have been successfully overcome, we are at a situation that in a span of around 15 years, SiMOSFETs can be scaled no more, nor can we be able to improve performance by clever changes in Fabrication. A number of alternate devices have been reviewed, researched and tested and only a few of these new devices come close to the flexibility and potential that SiCMOS offers. Two Devices which stand out as replacements are Carbon nanotube field effect transistors (CNTFET) and Single Electron Transistors (SET). These devices has some properties that are mandatory for a logic device and some properties that are absent. This paper analyses the strengths and weaknesses of these devices as replacement for SiMOSFETs.

II. CARBON NANOTUBE FIELD EFFECT TRANSISTORS

A. CNTFET Concept

Nanometer-diameter single-walled carbon nanotubes (SWNTs) exhibit unique electronic, mechanical, and chemical properties that make them attractive building blocks for molecular electronics. Depending on diameter and helicity, SWNTs behave as one-dimensional metals or as semiconductors, which, by virtue of their great mechanical toughness and chemical inertness, represent ideal materials for creating reliable, high-density device.

In the past few years, various basic single-nanotube components have been demonstrated, such as molecular wires, diodes, field-effect transistors, single-electron transistors, and cross bar memories. The next challenge in the development of molecular electronics is to go beyond single-molecule components and integrate such devices onto a chip to demonstrate digital logic operations. Fig.1 shows a state-of-the-art CNTFET.

Fig.1. Device layout. (A) Height image of a single-nanotube transistor, acquired with an atomic force microscope. (B) Schematic side view of the device. A semiconducting nanotube is contacted by two Au electrodes. An Al wire, covered by a few-nanometers-thick oxide layer, is used as a gate. (C) Height-mode atomic force microscope image of two nanotube transistors connected by a Au interconnect wire. The arrows indicate the position of the transistors.
For CNTFET, the resistivity is constant with size, which is more desirable than Si-MOSFET, since the resistivity changes drastically at small dimensions in the latter case. Thus, CNTs make excellent interconnects. Experiments have already shown that CNTFETs may have good on-off current ratio and fair gain. They work under room temperature.

All above the merits of CNTFET. At the same time, some issues must be considered in the research. The electrical properties of CNTFETs can be drastically altered by adjusting a number of device parameters. These parameters include contact (gate, source, drain, etc.) material and annealing temperature. In order to properly utilize these advanced properties, devices must be designed to take advantage of all device parameters and still be conducive to the consistent formation of carbon nanotubes, thereby requiring a more exact manufacturing process.

A common feature of the SWCNTFET fabricated has been the presence of a Schottky barrier at the nanotube-metal junctions. These energy barriers severely limit transistor conductance in the “ON” state, and reduce the current delivery capability. This problem can be solved by choosing appropriate contact material. Using palladium, a noble metal with high work function and good wetting interactions with nanotubes, greatly reduces or eliminates the barriers for transport through the valence band of nanotubes. The size of the transistor is so big (L=3um or 0.3um) that it needs more effort to apply it to real application. Fig.2 and Fig.3 show the layout and electrical properties curves of this transistor.

Fig.3. Room-temperature electrical properties of high-performance SWNT-FETs ($t_{ox} = 67$ nm).

Many other research directions were taken on CNTFETs. For example, a framework for self-assembly of carbon nanotube–based electronics using DNA and homologous genetic recombination was presented by Keren and his colleagues.

The problems bothering the CNTFETs research are listed below: Consistently high background noise is one of the biggest problems for the CNTFET performance. The operation frequency is limited due to parasitic capacitance and huge external resistance. High off current and large leakage are big issues considering the power consumption. While commercial access to MWNT is less problematic, all currently known synthesis methods for SWNTs result in major concentrations of impurities. These impurities are typically removed by acid treatment, which introduces other impurities.

Fig.2. Pd-contacted long ($L = 3 \mu m$) and short ($L = 300 \text{ nm}$) back-gated SWNT devices formed on the same nanotubes on SiO$_2$/Si.

Fig.4. A DNA-templated carbon nanotube FET and metallic wires contacting it. SEM images of SWNTs contacted by self-assembled DNA-templated gold wires. (A) An individual SWNT. (B) A rope of SWNTs. Bars, 100 nm.
that can degrade nanotube length and perfection, and adds to nanotube cost. Another problem, especially for electronic devices, is that the usual synthetic routes result in mixtures of various semiconducting and metallic nanotubes. Metallic SWNTs can be selectively destroyed by electrical heating, so that only the semiconducting nanotubes needed for nanotube field-effect transistors (NT-FETs) survive. However, no route to substantial quantities of SWNTs of one type is yet known.

III. Single Electron Transistors

Single Electron Devices are based on the principle of Coulomb blockade explained above. Any movement of electrons through the dots requires the integer number of electrons in the dot to change by one. But, due to the repulsive forces between the electrons, the energy of the dot containing N+1 electrons will be higher than the energy of the dot containing N electrons. This extra energy needed to increase the electron number by 1 must be supplied by increasing the external voltage, thereby allowing current to flow. This principle is known as Coulomb blockade[3]. By controlling the external voltage, the tunneling in the device is controlled. The external voltage should provide the necessary addition energy, $E_a$, which is needed to increase the number of electrons by 1. The addition is given by the simple formula:

$$E_a = E_c + E_k$$  

Here $E_k$ is the quantum kinetic energy and $E_c$ is the charging energy given by:

$$E_c = \frac{e^2}{C}$$

An important condition for a Coulomb Blockade device is that the $E_c \gg k_bT$ (3)

For an island of size $\sim 100\text{nm}$, $E_a$ is dominated by $E_c$. Fig[5] shows the variation of energy with diameter. $E_a$ approaches 1meV, i.e., $\sim 10\text{ K}$ in temperature units when the size of the dot is $\sim 100\text{ nm}$. But due to thermal fluctuations, the operating temperature has to be less than 1 K for the single electron effects to be visible. Single electron devices suggested for digital circuits need an $E_a$ of a few electron volts and for these circuits to work at room temperature, the size of the dot must be $\sim 1\text{ nm}$[5]. This is the biggest challenge that needs to be addressed for this technology to be the technology of the future.

Fig 5. Single-electron addition energy $E_a$ (solid line), and its components: charging energy $E_c$ (dashed line) and electron kinetic energy $E_k$ (dotted line), as calculated using Equations (1) and (2) for a simple model of a conducting island[5].

Another Condition that needs to be adhered to, in order to observe coulomb blockade is that the resistance $R_t$ of the tunneling junction must be larger than resistance quantum $\hbar/e^2$.

$$R_t \gg \frac{\hbar}{e^2} = 25.8\text{ k}\Omega$$ (4)

This relation is of principal importance for single-electrons as a whole.

A. Single Electron Transistors

Single Electron Transistors are based on the principle of Coulomb blockade explained above. The construction of a single electron transistor is shown in Fig[6]. The device has an island of either Al/Ti/Si with a source electrode and a drain electrode on either side of the dot. The Source and drain electrodes form the tunneling contacts and are separated from the dot by a thin oxide layer. The gate electrode is separated from the dot by a thick oxide layer. The arrangement of the Gate, source and drain electrodes resemble a SiMOSFET.

Fig. 6. Construction of a Single Electron Transistor

By inducing a non-integral number of charge in the gate, the number of electrons in the gate can be increased by 1. When the
charge on the gate is \( n \) then the charge on the dot can only be \( n \). If the charge on the gate is \( (n + 1/2) \), then the charge on the dot can be \( n \) or \( n + 1 \). When the charge on the dot changes from \( n \) to \( n + 1 \), current flows through the device. The fig[7] shows the variation of charge in the dot due to the gate voltage \( V_g \).

The variation of tunnel current with gate voltage is shown in fig[8]. Each peak corresponds to the voltage at which 1 electron is added to the dot. The distance between peaks is proportional to the addition energy needed to add an electron to the dot.

Fig[9] shows the I-V curves of a single electron transistor. As these curves are continuous, the gain and transconductance at any given current value may either be negative or positive based on the gate voltage at that instant. This is a marked difference between the I-V curve of a SiMOSFET and that of a SET.

![Fig. 7. "Coulomb staircase", i.e. the step-like dependence of the average charge \( Q \) of the island on the gate voltage \( V_g \), for several values of temperature.](image)

![Fig. 8. the Coulomb oscillations in the current vs. gate voltage for a 0.5 mm diameter dot[4].](image)

Fig. 9. I-V curve of a SET

**B. Comparison of a SET with a SiMOSFET**

Fig[10] compares a SiMOSFET with a SET based on several qualitative and quantitative parameters. The Primary Advantages of SETs over a SiMOSFET are:

1. Low Power Dissipation
2. Packing Density is extremely high.
3. Scalable i.e., performance can be improved by decreasing size.

Although, these are exactly the reasons why the industry is looking for an alternative to SiMOSFET, the disadvantages of SETs overshadow their advantages. A few reasons, why SETs cannot replace SiMOSFET:

1. The Fan-out of the single electron transistor is very poor due to very low currents (3 nA). The on – off ratio is also very poor making it a poor choice for designing static circuits.[12]
2. In order to reduce the effects of background charge fluctuations, the critical dimensions of the SETs must be in the order of 2 nm. Unless significant progress is made in controlling these effects, it seems unlikely that Coulomb blockade circuits can be integrated on a large scale.
3. Although static leakage currents are low, the power density of these devices at room temperature are greater than 10 kW/cm\(^2\) for a circuit with more than 10\(^{11}\) devices. This does not pose a big challenge to CMOS[8].
4. These devices have very poor tolerance to manufacturing errors. A small change in critical dimensions of these devices affects their operation drastically. Hence, an extremely precise fabrication process is needed. Thus, the startup cost and also, the cost/device may be much higher than that of a SiMOSFET.

5. SiMOSFETs had a lot of “room at the bottom”[13]. SETs start at a size of close to 100nm and probably will scale only for 2 generations before which the
lithography challenges will again be met. A dramatic scaling for over 8 generations by SiMOSFETs is not possible by SETs and hence, will not serve the purpose as a long-term replacement for CMOS.

6. The Operating temperature for the SETs to work with considerable gain is less than 1K for a dot size that can be fabricated with the current technology. The highest temperature for which the gain is a value of 5.2 is 250mK. These low operating temperatures are impossible on a large scale, thus making SETs infeasible to manufacture commercially.

IV. CONCLUSION

For the research of CNTFET, the challenge existing in the development of molecular electronics is to go beyond single-molecular components and integrate such devices. Present research shows strong promises of this new nano-technology. But at the same time, there’re still many things we need to consider. Though CNTFETs may be a very probable replacement for Si-MOSFET in the future, we don’t see much advantage of CNTFETs over Si-MOSFET at present.

As far as SETs go, The merits of SET are completely overshadowed by its drawbacks as a logic device. There are numerous problems in SETs that must be addressed before it is even considered as a replacement “logic device” for SiMOSFET. These problems are resolved at a great expense and the results shown by SETs today are not promising enough to invest in fabricating them on a large scale. There has been very little progress made in designing a completely logic out of SETs. The most advanced circuit being the Inverter. Thus, a complete logic structure with only SETs that is as robust as a SiMOSFET circuit is infeasible and virtually impossible as of today.

REFERENCES