

# DEAN RYAN MORRISON

**CURRENT RESIDENCE**  
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**PERMANENT RESIDENCE**  
10450 SW 96 Terrace  
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- Objective** To obtain full-time employment in an engineering field related to computer architecture, digital design, or digital system architecture. Available Feb. 2007
- Education**
- Master of Science in Electrical Engineering** Dec. 2006  
University of Florida  
**GPA: 3.68** (33 credit hours)  
Emphasis: Computer Architecture and Digital Design
- Bachelor of Science in Computer Engineering, Summa Cum Laude** May 2005  
University of Florida  
**GPA: 3.8** (143 credit hours)  
Minor in Mathematics
- Advanced Courses**
- Hardware:** Virtual Computers, Parallel Computer Architecture, Digital Computer Architecture, Digital Design, Advanced VLSI Design
- Software:** C++ Programming, Data Structures and Algorithms, Operating Systems, Software Engineering
- Mathematics:** Probability Theory and Stochastic Processes, Numerical Analysis
- Communications:** Digital Communications, Noise in Linear Systems
- Research**
- Simulator Design for Custom CMP Cache Hierarchies
  - Dynamically Optimized Cache Sharing for CMP Architectures
  - Dynamically Adaptive Prepaging for Effective Virtual Memory Management
  - Value Prediction Methods for Superscalar Pipelined Architectures
- See <http://plaza.ufl.edu/dean8201/myweb/samples%20of%20my%20work.htm>
- Work Experience**
- Harris Corporation** – Palm Bay, FL Summer 2006  
*Intern: ASIC and Aerospace Processing*
- Designed a Signal Integrity Analysis procedure for use in the development of layout and routing constraints for circuit card assemblies
  - Supported the development of FPGA interface architectures and protocols
- University of Florida** – Gainesville, FL Fall 2005, Spring 2006  
*Teaching Assistant: EEL4712 Digital Design*
- Instructed three 3-hour labs per week, providing guidance to students in VHDL design, design verification, and FPGA emulation
- Honeywell International** – Clearwater, FL Summer 2004, Summer 2005  
*Intern: Aerospace Electronic Systems - Electrical Design*
- Performed pre-layout and post-layout signal integrity analysis
  - Performed worst case decoupling analysis for Xilinx FPGAs
- Florida Power and Light** – Miami, FL Summer 2003  
*Intern: Transmission Operations and Planning*
- Integrated database queries and spreadsheets to track equipment operation
- Skills**
- Simulation Tools:** Simics, SimpleScalar, Cadence, ICX, SigXP, Allegro
- Hardware Tools:** Xilinx Virtex-II Pro FPGA, Altera Cyclone FPGA, Altera CPLD, Motorola 68HC12, TI MSP430
- Software Tools:** Altera Quartus, Visual Studio 6.0, MATLAB
- Coding Languages:** Perl, VHDL, C, C++, Java, Motorola Assembly, MIPS Assembly, Oracle SQL
- Operating Systems:** Windows, Unix, Solaris