Design and Evaluation of a Low-Power UART-Protocol Deserializer

Casey T. Morrison, William Goh, Saeed Sadrameli, and Eric Blattler

***Abstract*—The design and evaluation of a low-power Universal Asynchronous Receiver/Transmitter (UART)-protocol deserializer is presented. Three separate techniques are employed to reduce power consumption on this, a common device used in serial communications: (1) State-machine-controlled global clock gating, (2) data-dependant local clock gating, and (3) low-V_{DD} supply. The benefits of employing all three techniques are quantified over a range of parameters. Comparisons are made between this design and one that does not implement the aforementioned power-reducing techniques.**

***Index Terms*—Low-power, UART, clock gating, NC2MOS**

I. Introduction

THE design of low-power data paths is a well-studied topic with major implications, especially for portable or high-performance applications. Several techniques for low-power design have been proposed and evaluated by [1] and [2], including parallel data paths, supply voltage scaling, and gated clocks. Many of these techniques have been shown to produce marked power savings, especially when used in conjunction with other techniques. In addition, several novel low-power flip-flop designs have been proposed. One such design, [3], is utilized in this paper as a means to implement local clock gating. This technique is used in conjunction with state-machine-controlled global clock gating and a low-V_{DD} supply to minimize power dissipation in the target design.

This three-fold power reduction technique is applied to a UART-protocol deserializer. UART serializers and deserializers are common devices used in many applications requiring a serial interface. Most microcontrollers are designed to have at least one UART interface. One obvious application for the low-power UART design proposed in this paper is in ultra-low-power sensor devices. Battery-powered sensors must acquire and transmit data (often serially) with minimal power consumption. As an Intellectual Property (IP) core or as a stand-alone device, the design presented in this paper takes steps towards significantly reducing the power consumption for a UART serial interface.

As with most power-reducing techniques, there exist tradeoffs in this design. A power reduction of more than 55% can be achieved with a limited increase in area and delay. While the area, delay, and power tradeoffs presented in this paper may be acceptable for the targeted application, this may not be the case for other applications.

II. Architecture and Design

This design explores the effects of a hierarchical approach to power reduction. Different techniques are employed at different levels of the design hierarchy.

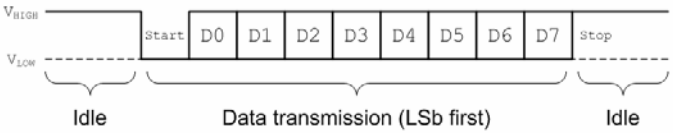

Fig. 1. UART serial communication protocol with eight data bits, no parity, one start bit, and one stop bit.

TABLE I
Physical and Electrical Specifications

Parameter	Value
V_{DD}	$1.5\ V \le V_{DD} \le 2.5\ V$
Technology	TSMC 0.25 μm Deep Submicron
Supported baud rates	All standard baud rates up to 41.67 Mbaud
Input clock frequency	$2.4\ KHz \le f_{CLK} \le 333.3\ MHz$
Clock duty cycle	50%
Core logic dimensions	163.68 μm x 114.72 μm = 0.0188 mm^2
Total die dimensions	960.18 μm x 959.94 μm = 0.9217 mm^2
Number of pMOSFETs	720
Number of nMOSFETs	600

A. Specifications and Requirements

The design presented in this paper is a UART-protocol deserializer which can be used as the receiving end of a serial interface. The UART protocol is an asynchronous (i.e. clock-less) serial communications protocol. Fig. 1 shows the particular data format implemented in this design. Idle receive periods are characterized by a high receive signal. The start of a transmission is marked by a low "start bit" which is immediately followed by eight data bits, least-significant bit (LSb) first. The end of a transmission is marked by a high "stop bit." Some variations of this data format call for a parity bit immediately following the data bits, but no such feature is implemented in this design. The physical and electrical specifications for this design are listed in Table I.

B. Power Reduction Strategy

Three techniques for reducing power dissipation are utilized in this design.

1) State-machine-controlled global clock gating: The UART serial protocol lends itself well to state-machine-controlled global clock gating. When the serial receive input is idle (high) in between transmissions, there is no need to provide a clock to the majority of flip-flops in the deserializer circuit. The only flip-flops that require an uninterrupted clock are the receive detection flip-flops that constantly sense the receive input for an incoming transmission.

The state machine for the proposed deserializer is designed to cut off the clock signal to most flip-flops during the *Idle* state. When incoming data is detected (an event known as "RX detect"), the state machine then restarts the internal clock to process the received data. This technique inherently reduces power consumption during idle periods.

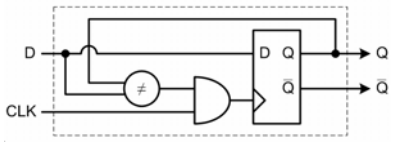

Fig. 2. Simplified functional diagram for the NC^{2}MOS flip-flop.

2) Data-dependant local clock gating flip-flops: The backbone of the deserializer is designed upon a novel NC^{2}MOS flip-flop [3]. NC^{2}MOS uses traditional master and slave latches with the addition of clock gating and a comparator. Fig. 2 shows a simplified functional diagram for this flip-flop. The comparator compares the output-Q with the input-D. When these signals are equivalent, the local clock is gated off. When the comparator detects a change, it generates a pulse for the master and slave latch to store the new output value. The flip-flop clock load is small as it only drives a single nMOSFET and pMOSFET. This design also requires no external clock inverter to drive the flip-flop. The design in [3] has been modified to be a positive-edge-triggered flip-flop with asynchronous set and clear.

The tradeoff of the NC^{2}MOS design is the layout area because it requires additional circuitry for the comparator and clock gating. Compared to a similar flip-flop design from the MOSIS standard cell library, the NC^{2}MOS flip-flop consumes 56.82% more area ($Area_{MOSIS}$ = 11,664 λ^2, $Area_{NC2MOS}$ = 18,291 λ^2). However, the NC^{2}MOS flip-flop has 72% less input clock load than its MOSIS counterpart. This reduction in clock load combined with the data-dependant local clock gating results in a significant decrease in average power consumption—one that is more pronounced as the activity rate for the flip-flop is decreased.

3) Low-V_{DD} supply: Lowering the power supply voltage quadratically reduces the dynamic power dissipation of the system according to the formula

$$P = C_L \cdot f \cdot V_{DD}^2 ,$$

where C_L is the capacitive load, f is the operating frequency, and V_{DD} is the supply voltage. It has been proposed by [5] that scaling the supply voltage as far down as 250 mV for a 0.25 µm technology produces the optimum energy-delay product. The side-effect of this technique is an increase in propagation delay. An increase in delay does not drastically impact this design for two main reasons. First of all, standard baud rates typically fall in the 300 baud to 2 Mbaud range, which translates to a relatively slow input clock frequency in the range of 2.4 KHz to 16 MHz. Secondly, most of the logic in this design runs from a divide-by-eight clock, which results in a relatively long computation time of about 60 ns – $T_{clk\text{-}q}$ – T_{setup}. The few paths that do run at the true input frequency have very little combinational logic in between flip-flops, so the increase in delay caused by reducing V_{DD} does not have a significant impact on the datapath delay.

C. High-Level Architecture

The proposed deserializer architecture was first implemented in Verilog HDL. Once simulations verified proper functionality, the design was then hand-translated into a graphical representation in Quartus design software using standard logic gates. Finally, once simulations re-affirmed proper functionality, the design was then implemented at the transistor level in Cadence.

This design consists of six modules: clock generation, receive detection (RX detect), receive state machine (RSM), receive shift registers (RSR), receive hold registers (RHR), and status signal generation. Fig. 3 illustrates the high-level architecture of this design.

The serial receive input is constantly sampled by the RX detect circuit, and when an incoming data transmission is detected, the RSM will transition from the *Idle* state to the *Shift* state. While in the *Shift* state, data on the RX input is serially shifted into the RSR. Once eight bits of data is shifted in, the RSM transitions to the *Load* state in which data is transferred in parallel from the RSR to the RHR, and the RXRDY flag is asserted high. Data in the RHR is asserted on the DATA[7..0] bus when the active-low READN signal is asserted. If this does not occur before the next transmission is received, then an OVERRUN error will be asserted indicating that the RHR has been corrupted with new data.

D. Physical Design

The physical design of this deserializer was carried out in a structured and consistent manner, using many of the conventions suggested by [6] and [7]. The layout is partitioned according to Fig. 5. As a stand-alone integrated circuit (IC), this design is heavily I/O-bound in terms of the die area. With fourteen pins, the area enclosed by the pad frame is significantly larger than the area required for the logic. As a hard macro IP, the design is fairly compact and can easily be integrated into larger-scale layouts.

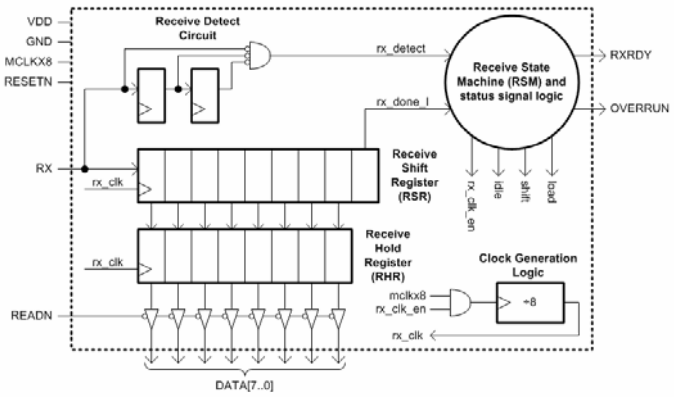

Fig. 3. Top-level architecture for a low-power UART-protocol deserializer.

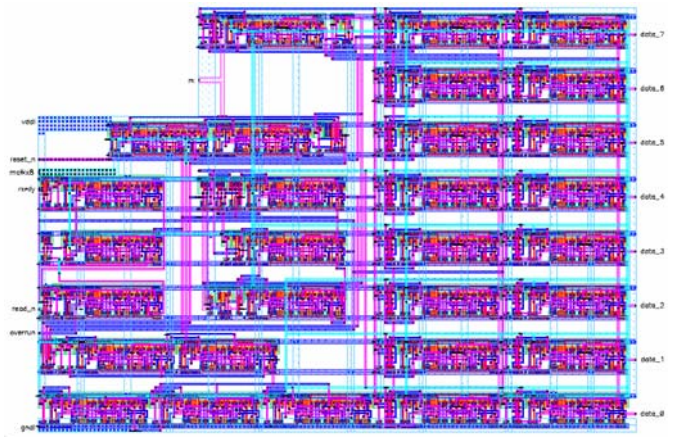

Fig. 4. Low-power deserializer core logic layout.

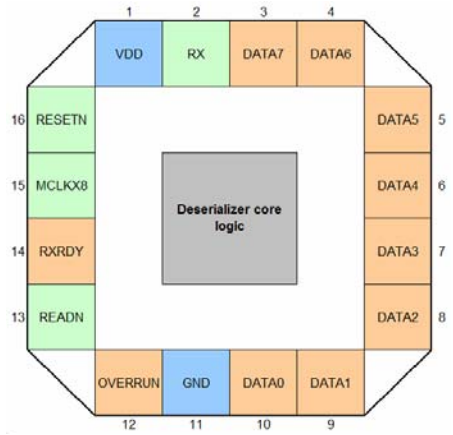

Fig. 5. I/O positions relative to the core logic layout. Green pads represent inputs, red pads represent outputs (or bi-directional I/Os), and blue pads represent supplies.

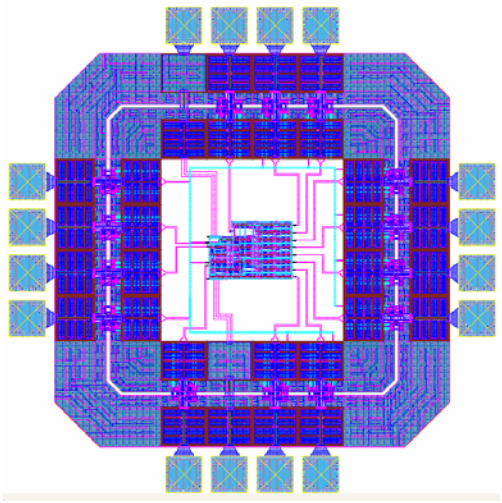

Fig. 6. Low-power deserializer layout with I/O pad frame.

III. Design Evaluation

The proposed deserializer design was evaluated using a combination of functional tests and performance characterizations. In addition to module-level simulations, design rule checking (DRC), and layout versus schematic (LVS) checking, extensive simulations were conducted at the top level.

A. Functional Verification

To ensure a functionally sound circuit, this design was simulated over a range of input combinations. Fig. 7 shows a functional simulation during which two separate serial transmissions are received. This waveform demonstrates proper functioning of the RXRDY and OVERRUN status signals, as well as the state-machine-controlled global clock gating. After the second transmission is received, the internal clock (RX_CLK) is turned off, and the OVERRUN error is asserted indicating that the second byte that was received has overwritten the first.

B. Power Analysis

To evaluate the power performance of this design, a control design was used as a baseline for comparison. The control design is functionally identical to the proposed design, except it does not implement either of the clock gating techniques utilized in the proposed design. Instead of using the NC^{2}MOS flip-flop, the control design uses a standard flip-flop from the MOSIS SCMOS standard cell library. In addition, the control deserializer does not implement any clock gating during the *Idle* state.

Each design is simulated for different levels of signal activity and for different values of V_{DD}. The activity rate, α, used in this analysis is defined as

$$\alpha = \frac{\text{active time}}{(\text{active time}) + (\text{idle time})},$$

where *active time* is the time during which the serial RX input is active, and *idle time* is the time during which the serial RX input is idle (high).

Different activity rates are achieved by adjusting the idle time between transmissions. In reality, serial communication lines experience varying degrees of idleness. The proposed design obtains its best power savings during periods of low activity, when the internal clock is shut down by the RSM.

Table II shows the results of the power analysis. Fig. 8 and Fig. 9 illustrate the dependence of power dissipation on activity rate and core voltage. As expected, the improvement in power dissipation achieved by the proposed design is most pronounced during low-activity periods. This trend is evident in Fig. 10. The control design is less dependant on activity rate since it does not implement clock gating during idle periods.

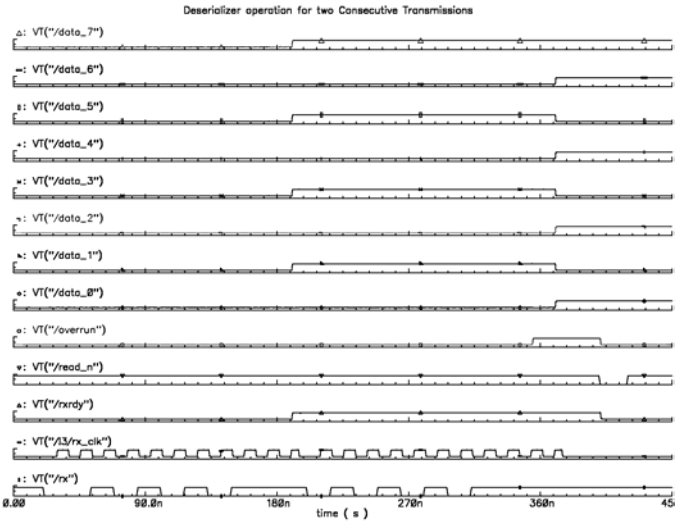

Fig. 7. Functional simulation waveform.

TABLE II
Simulation Results

Acivity rate	Core voltage	Total Energy for Low-Power design	Total Energy for Control design	Energy Difference	Total Power for Low-Power design	Total Power for Control design	Power Difference	Percent Energy/Power Improvement
α	V_{DD}	E_{low_power}	$E_{control}$	ΔE	P_{low_power}	$P_{control}$	ΔP	PI
[%]	[V]	[pJ]	[pJ]	[pJ]	[μW]	[μW]	[μW]	[%]
75%	2.5	0.920	1.043	0.123	230.010	260.763	30.753	11.79%
	2.1	0.698	0.699	0.001	146.630	146.872	0.241	0.16%
	1.8	0.571	0.585	0.013	102.816	105.233	2.417	2.30%
	1.5	0.449	0.417	-0.033	67.383	62.487	-4.896	-7.84%
60%	2.5	0.805	0.982	0.177	201.368	245.548	44.180	17.99%
	2.1	0.616	0.669	0.053	129.438	140.486	11.048	7.86%
	1.8	0.501	0.553	0.052	90.232	99.549	9.317	9.36%
	1.5	0.393	0.399	0.006	59.001	59.900	0.898	1.50%
45%	2.5	0.691	0.922	0.231	172.650	230.400	57.750	25.07%
	2.1	0.534	0.640	0.106	112.161	134.316	22.155	16.49%
	1.8	0.430	0.518	0.088	77.472	93.281	15.809	16.95%
	1.5	0.337	0.383	0.045	50.580	57.402	6.822	11.88%
30%	2.5	0.576	0.855	0.279	143.978	213.625	69.648	32.60%
	2.1	0.452	0.610	0.157	94.975	128.045	33.071	25.83%
	1.8	0.359	0.492	0.133	64.703	88.598	23.895	26.97%
	1.5	0.281	0.369	0.088	42.222	55.409	13.187	23.80%
15%	2.5	0.461	0.798	0.336	115.300	199.375	84.075	42.17%
	2.1	0.370	0.580	0.210	77.742	121.758	44.016	36.15%
	1.8	0.289	0.462	0.173	51.948	83.088	31.140	37.48%
	1.5	0.225	0.349	0.124	33.780	52.412	18.632	35.55%
0%	2.5	0.372	0.835	0.463	93.015	208.663	115.648	55.42%
	2.1	0.288	0.576	0.288	60.467	120.939	60.472	50.00%
	1.8	0.220	0.477	0.257	39.575	85.869	46.294	53.91%
	1.5	0.171	0.347	0.176	25.703	52.055	26.352	50.62%

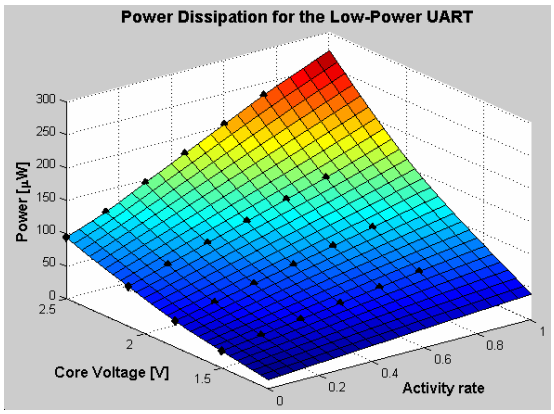

Fig. 8. Power dissipation for the proposed design versus core voltage and activity rate.

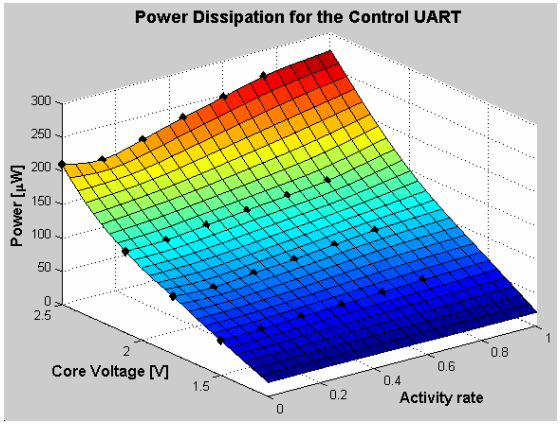

Fig. 9. Power dissipation for the control design versus core voltage and activity rate.

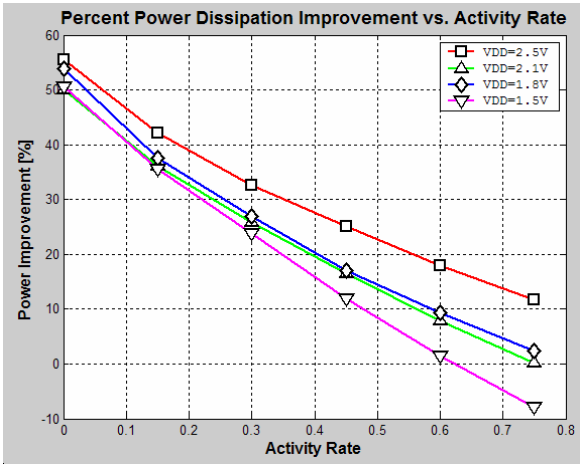

Fig. 10. Power dissipation improvement versus activity rate.

IV. Conclusions

This paper has demonstrated how a combination of techniques can yield significant power consumption reduction in a UART-protocol deserializer. Each technique, however, has a cost associated with it. Implementing state-machine-controlled global clock gating produces up to a 45% improvement in power consumption and requires only a small increase in area to implement the clock gating logic. Data-dependant local clock gating using NC^{2}MOS flip-flops can improve the power consumption by an additional 10-12% (see Fig. 11). However, this feature has a multiplicative cost associated with it, in that each flip-flop is about 57% larger compared to a standard design.

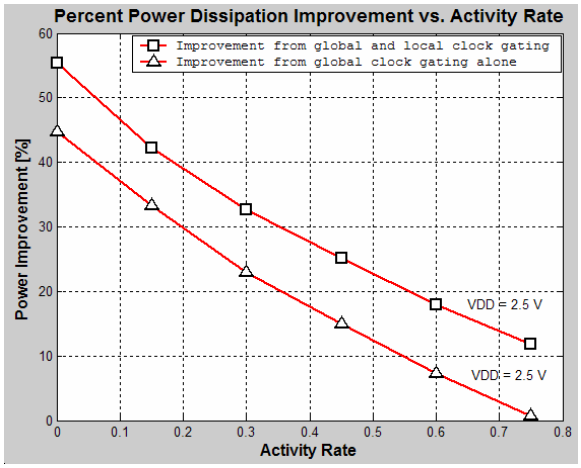

Fig. 11. Power dissipation improvement versus activity rate as different power-reducing features are added.

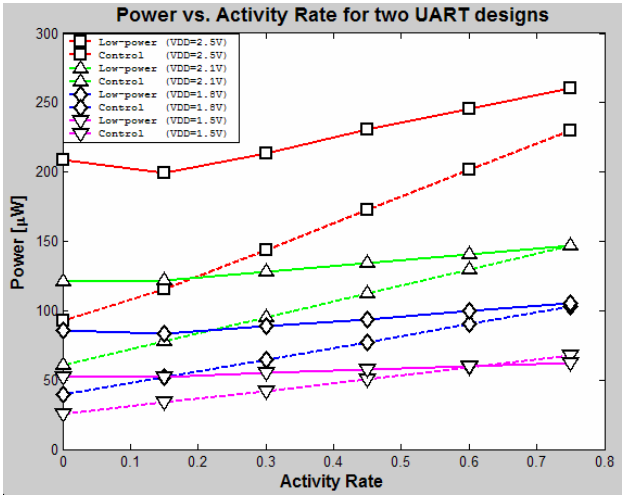

Fig. 12. Power dissipation for the two designs versus activity rate.

Although power dissipation is significantly reduced by lowering V_{DD}, it is worthwhile to note that the improvement in power dissipation achieved by the proposed design is 5-12% higher for high V_{DD} as compared to low V_{DD}. This indicates that supply scaling is more effective for the control design and only moderately effective for the proposed design.

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