ARNAV GUPTA

3800 SW 34th Street, Apt# DD298, Gainesville, FL, 32608 | +1(352)872-8644 | arnavgupta06@ufl.edu | http://plaza.ufl.edu/arnavgupta06/

OBJECTIVE

Seeking a summer internship where I may use my Computer Engineering skills to further company growth

EDUCATION

Master of Science in Electrical and Computer Engineering, GPA: 3.77/4.00 ***May 2016***
University of Florida, Gainesville, FL, USA
Courses: Computer Architecture, Reconfigurable Computing, VLSI Circuits and Technology

Bachelor of Technology in Electronics and Communication Engineering, CGPA: 8.2/10.0 ***July 2014***
Jaypee Institute of Information Technology, Noida, UP, INDIA
Courses: Digital Hardware Design, Microprocessors & Controllers VLSI testing, Digital Electronics, Semiconductor Devices

MAJOR PROJECTS

ARM Processor Synthetic Benchmark Development (*IDEAL Research Lab, UF. Advisor: Dr. Tao Li*) ***October 2014 – present***

- Working on first phase of the project where I statically cross compiled spec2006 benchmarks to ARMv8 board and collected performance counter statistics by means of Perf tool
- Used Valgrind to generate BBV for each benchmark in ARMv8 board and obtained simpoints and weights using SimPoint tool in host (Linux Ubuntu). Compared performance counters collected by Perf and SimPoint for verifying Simpoint
- Repeated same procedure for sysbench and fio benchmark.

FPGA Implementation of 1-D Time Domain Convolution (*UF, Advisor: Dr. Greg Stitt*) ***October 2014 – December 2014***

- Implemented convolution logic on FPGA board using VHDL, which exploits a significant amount of parallelism to provide better performance than microprocessor

Design and Simulation of Virtual Reconfigurable Circuits for Fault Tolerant Systems ***July 2013 – May 2014***

- Developed a 4x3 grid of reconfigurable programmable elements and mapped onto FPGA using configuration bit-stream which was created using Cartesian Genetic Programming. Project was coded at gate level in Verilog HDL
- Complete hardware implementation was evolved when 100% fitness achieved by the new configuration bit-stream

Applications of MFCC and Vector Quantization in Speaker Recognition ***July 2012 - December 2012***

- Improved speaker recognition systems to achieve the recognition rate of 89% and reduce the distortion upto 69%
- Optimized MFCC for feature extraction and Vector Quantization (VQ) for feature modelling and coded in MATLAB

WORK EXPERIENCE

Research Assistant, IDEAL Research Lab, University of Florida ***October 2014 – present***

- Working on ARM processor synthetic benchmark development project listed in '*Major Projects*' section above.

Intern, Indian Railways ***May 2013 – July 2013***

- Researched the Control, Exchange, UTS and Railnet departments of Indian Railways
- Closely understood the man and machine interaction in the proper functioning of the India's one of the largest industry

Intern, CETPA Infotech Pvt. Ltd., India ***December 2012-January 2013***

- Completed the formal training in VLSI design by gaining practical and theoritical expertise in Verilog HDL and VHDL

PUBLICATIONS

- **Design and Simulation of Virtual Reconfigurable Circuits for Fault Tolerant Systems:** *Presented in International Conference- ICRAIE 2014, published in IEEE Xplore Digital Library, ISBN: 978-1-4799-4041-7*
- **Applications of MFCC and Vector Quantization in Speaker Recognition:** *Presented in International Conference- ISSP 2013, published in IEEE Xplore Digital Library, ISBN: 978-81-909376-6-5, pp-178-181*

CERTIFICATIONS

- National Instruments Certified LabVIEW Associate Developer(CLAD) (No:100-314-6872) ***November 2014 – present***
- Certified Verilog HDL Designer (License: NVer141220124W643124) ***December 2012 – present***
- Certified VHDL Designer (License: NVHD141220124W512825) ***December 2012 – present***

SKILLS

Hardware Skills : VHDL, Verilog, RTL design, Logic Synthesis, Layout in CAD tools, DRC, LVS
EDA Tools : Xilinx ISE, Virtuoso, Spectre, Modelsim, PSpice
Software Skills : C/C++, UNIX, MATLAB, LabVIEW, Simple Scalar, Simpoint, Perf, Valgrind

LEADERSHIP

- **Vice President**, Rotaract Club Delhi Vikas, New Delhi ***October 2013 – May 2014***
- **Volunteer, Indian Grand Prix,** Jaypee Sports International Limited ***October 2012***